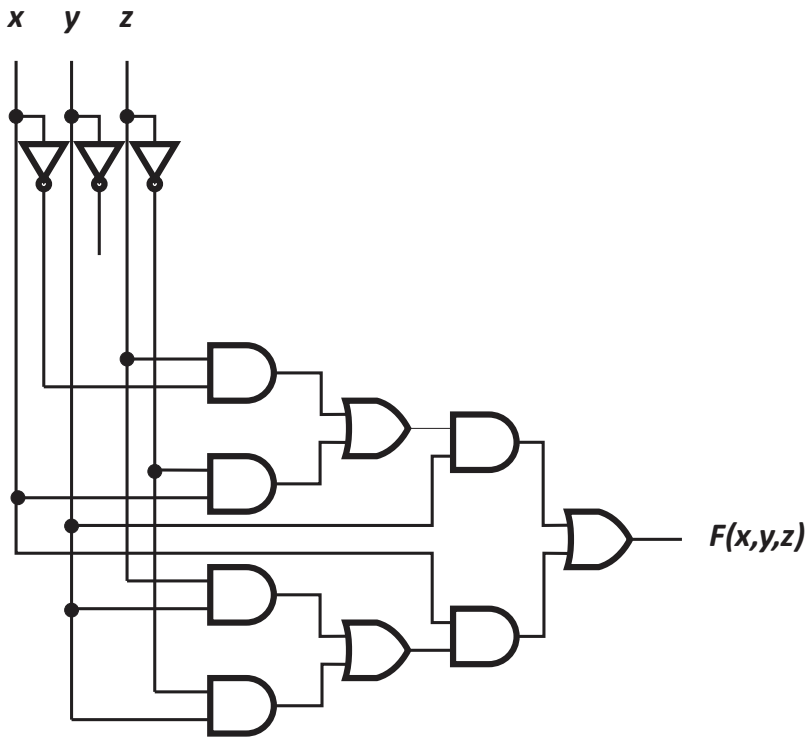
1. Print your name on your SCANTRON in the space labeled **NAME**.
2. Print **CMSC 2833** in the space labeled **SUBJECT**.
3. Print the date **12-9-2019**, in the space labeled **DATE**.
4. Print your **CRN, 10839,** in the space labeled **PERIOD**.
5. Print the test number and version, **T3/V2**, in the space labeled **TEST NO.**
6. This is a closed-book examination. No reference materials are permitted. No notes are permitted.
7. You may not consult your neighbors, colleagues, or fellow students to answer the questions on this test.
8. Cellular phones are prohibited. The possessor of a cellular phone will receive a ***zero*** (***0***) if the phone rings or is visible during the test.
9. You may use your personal calculator on this test. You are prohibited from loaning your calculator or borrowing a calculator from another person enrolled in this course.
10. Mark the best selection that satisfies the question. If selection **b** is better that selections **a** and **d**, then mark selection **b**. Mark only ***one*** selection.
11. Darken your selections completely. Make a heavy black mark that completely fills your selection.
12. Answer all **50** questions.
13. Record your answers on SCANTRON form **882-E (It is green!)**
14. When you have completed the test, place your SCANTRON, face up, between pages 2 and 3 of your questionnaire and submit both the questionnaire and your SCANTRON to your instructor.

1. Find the truth table for function F whose logic diagram is given below.



x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

a.

x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

b.

x	y	z	F
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

c.

x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

d.

2. To what power of 10 does the prefix micro- refer? What is the (approximate) equivalent power of 2?
   a. $1Ms = 10^6 s \approx 2^{20} s$
   b. $1\mu s = 10^{-6} s \approx 2^{-20} s$
   c. $1ms = 10^{-3} s \approx 2^{-10} s$
   d. $1ks = 10^3 s \approx 2^{10} s$

3. Convert 3654.9716_{10} to hexadecimal.

   a. $E46.F8BA$
   b. $64E.F8BA$
   c. $E46.F879$
   d. $AAE.978F$

4. Convert $EXAM.HELP_{36}$ to decimal.

   a. 1252618.81697543
   b. 1252619.81697534
   c. 696334.48348968
   d. 1252618.81697534

5. Express 321_{10} in a 12-bit one's complement representation.

   a. 1110 1011 1110
   b. 1001 0001 0010
   c. 1101 1110 0110
   d. 0001 0100 0001

6. Add 229_{10} to -254_{10} using 12-bit one's complement arithmetic.

   a. $FE6_{16}$
   b. 019_{16}
   c. 025_{16}
   d. 154_{16}

7. Which of the following pairs consisting of inventor, invention is incorrect?

   a. Charles Babbage, Difference Engine
   b. Konrad Zuse, Z1
   c. Seymour Cray, CDC 6600
   d. John Mauchly, GENIAC

8. Express -387_{10} using 12-bit two's complement arithmetic.

   a. 183_{16}
   b. $E7D_{16}$
   c. $E7C_{16}$
   d. 381_{16}

9. During the first pass of an assembler:

   a. the symbol table is only partially completed
   b. addresses from the symbol table are placed in object code
   c. external code is merged with the object code
   d. instructions are only partially assembled

10. Subtract 419_{10} from 320_{10} using 12-bit two's complement arithmetic.

    a. 1111 1001 1101
    b. 1110 0101 1101
    c. 0001 1010 0011
    d. 0001 0100 0000

11. The third generation of computers was characterized by the
    a. Introduction of the transistor
    b. Introduction of single-chip computers
    c. Introduction of integrated circuits
    d. Introduction of minicomputers.

12. Select the Figure that correctly computes the unsigned binary product of 5×13.

```
      1 1 0 1
    X   1 0 1
    -----------
      1 1 0 1
    1 1 0 1
    -----------
  1 0 0 1 1 1
```

Figure a

```
        1 1 0 1
      X   1 0 1
    -------------
        1 1 0 1
    1 1 0 1
    -------------
1 0 0 0 0 0 0 1
```

Figure b

```
      1 1 0 0
    X   1 0 1
    -----------
      1 1 0 0
  1 1 0 0
  -----------
1 1 1 1 0 0
```

Figure c

```
        1 1 0 1
      X   1 0 0
    -------------
        0 0 0 0
      0 0 0 0
    1 1 0 1
    -------------
  1 1 0 1 0 0
```

Figure d

13. Compute the quotient and remainder modulo 2 of $97 \div 13$.

	Quotient	Remainder
a.	111	110
b.	1010	001
c.	1001	100
d.	1000	000

14. Find the IEEE-754 single binary representation in hexadecimal of 37.5_{10}.

    a. 44160000
    b. 42180000
    c. 42480000
    d. 42160000

15. Which of the values below can be converted to this IEEE-754 single binary value, $\boldsymbol{66FF0C2F}$, in hexadecimal representation?

    a. 6.0221×10^{23}
    b. 2.9979×10^{8}
    c. 1.602284×10^{-19}
    d. 9.8

16. Which of the following messages, M, that were received, have no errors given polynomial $P = 1011$ was used to create M.

    a. 1001101111
    b. 1101101011
    c. 1101111111
    d. 1101101111

17. Which truth table specifies function $f(x, y, z) = yz + z(xy)'$?

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

a.

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

b.

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

c.

x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

d.

18. Using DeMorgan's Law, select the expression that is the complement of $f(x, y, z) = (x' + y)(x + z)(y' + z)'$?

    a. $f'(x, y, z) = x' + y' + z'$
    b. $f'(x, y, z) = x' + y + z$
    c. none
    d. $f'(x, y, z) = x' + y' + z$

19. Which of the following is NOT equivalent to $f(w, x, y, z) = (w + x + z')(w + x' + z)(x' + y + z)(x + y + z')$?

    a. $f(w, x, y, z) = x'z' + xz + wy$
    b. $f'(w, x, y, z) = \sum(0,2,5,7,8,10,11,13,14,15)$
    c. none
    d. $f'(w, x, y, z) = w'x'z' + w'xz + wxz + wxy + wx'z' + wx'y$
       $f(w, x, y, z) = w'x'z' + w'xz + wxz + wxy + wx'z' + wx'y$

20. Simplify $f(x, y, z) = xyz'' + (y + z)' + x'yz$ using Boolean algebra and its identities.

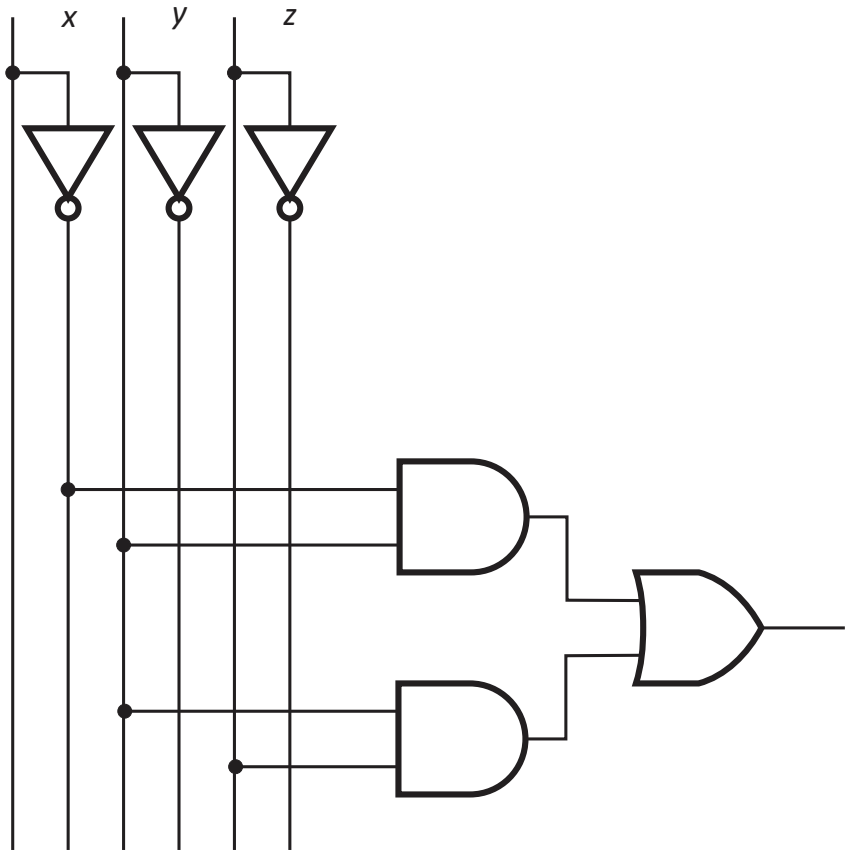
    a. $f(x, y, z) = (y \oplus z)'$
    b. $f(x, y, z) = (y \oplus z)$
    c. $f(x, y, z) = (x \oplus y)'$
    d. none

21. Select the expression for $f(x, y, z)$, in sum-of-products form, NOT simplified, given by the truth table shown.

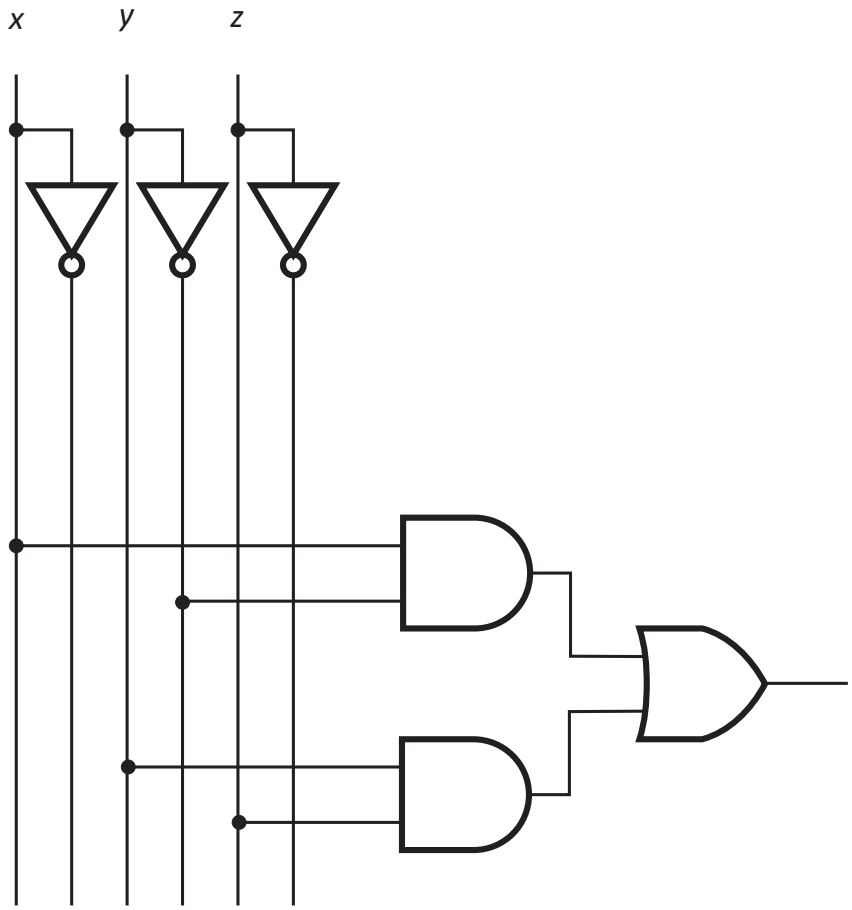
x	y	z	f
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

    a. $f(x, y, z) = (x + y + z')(x + y' + z')(x' + y + z)$
    b. $f(x, y, z) = x'z' + xy + xz$
    c. $f(x, y, z) = x'z' + yz' + xz$
    d. $f(x, y, z) = x'y'z' + x'yz' + xy'z + xyz' + xyz$

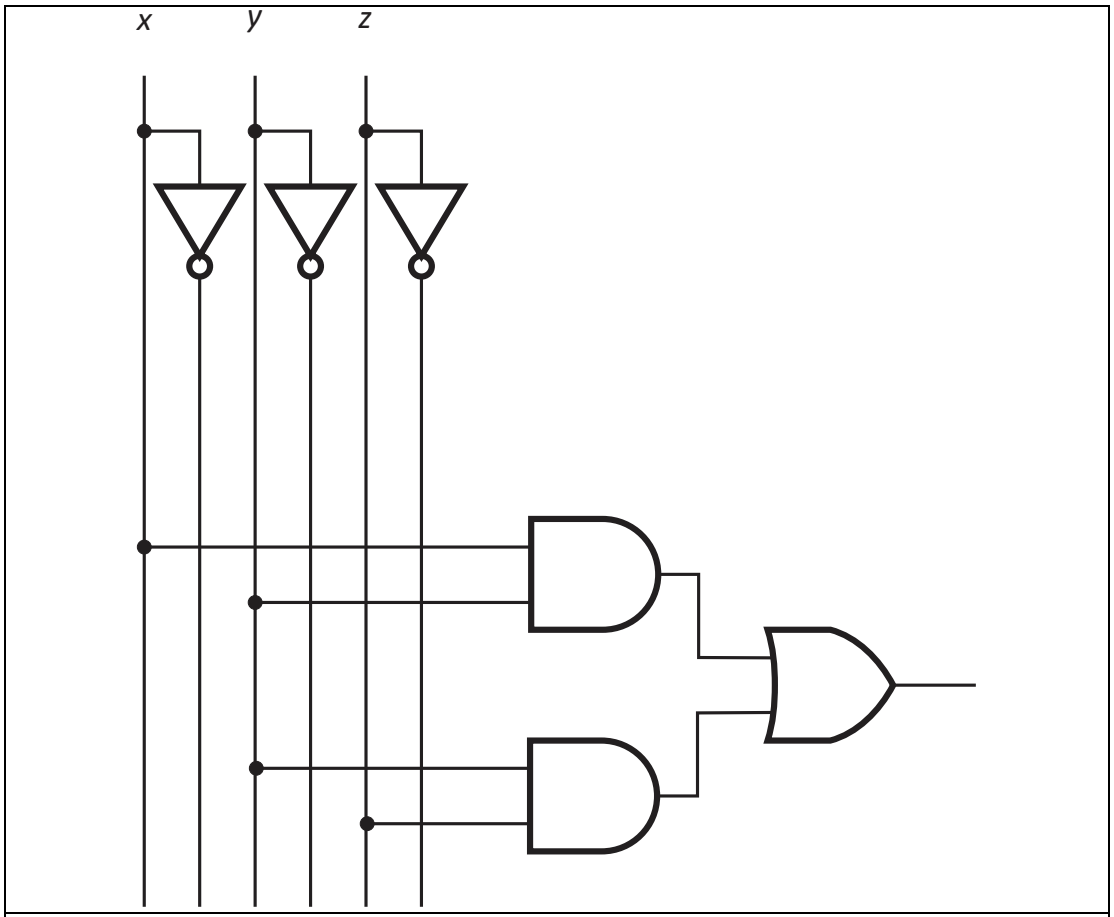
22. Select the logic diagram that implements simplified expression for $f(x, y, z) = y(x'z + xz') + x(yz + yz')$.



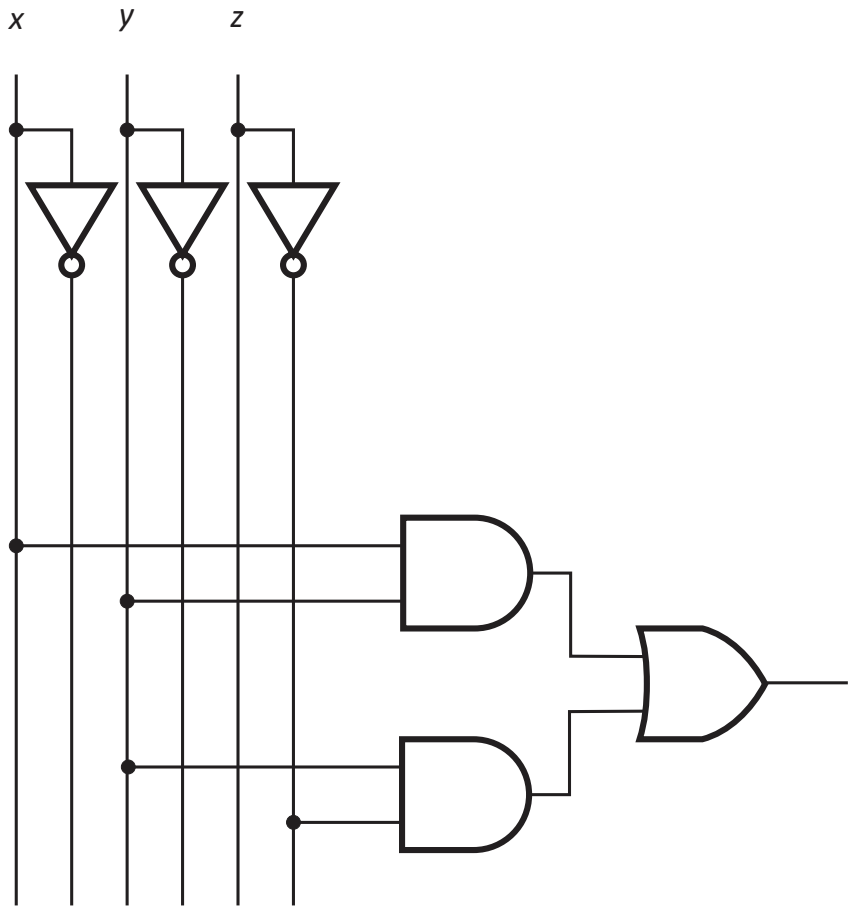
a.



b.



c.



d.

23. Select the truth table that specifies a full adder given x is the augend, y is the addend, z is the carry-in, c is the carry-out, and s is the sum.

x	y	z	c	s
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

a.

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

b.

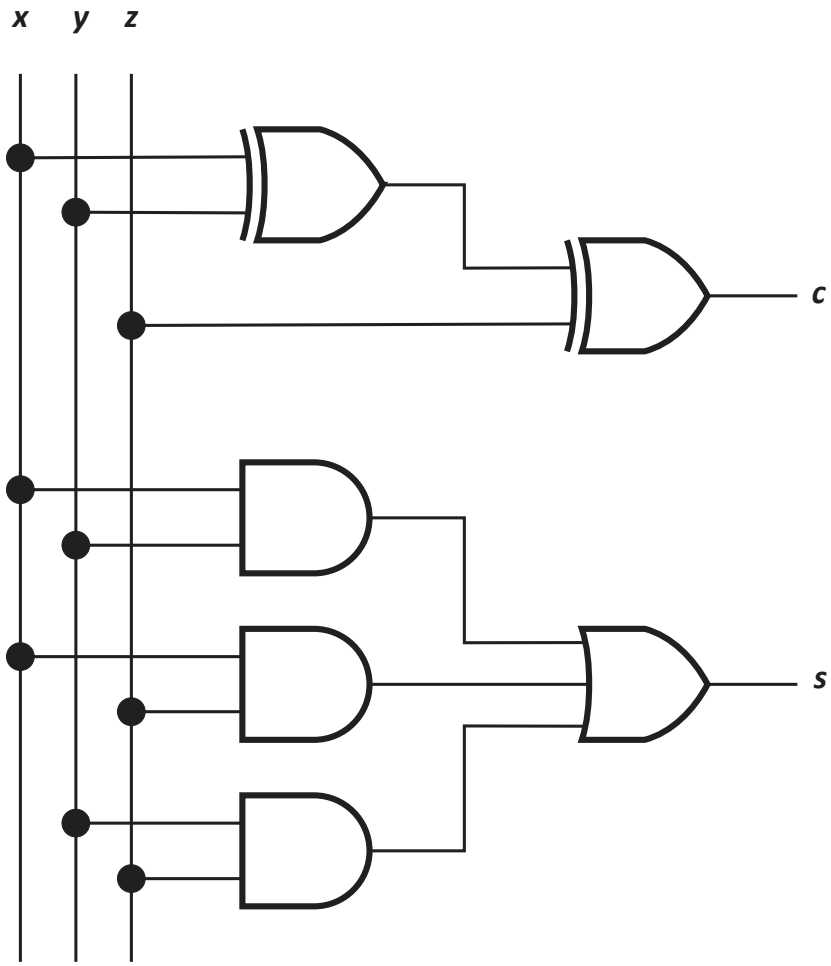
x	y	z	c	s
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	0	1

c.

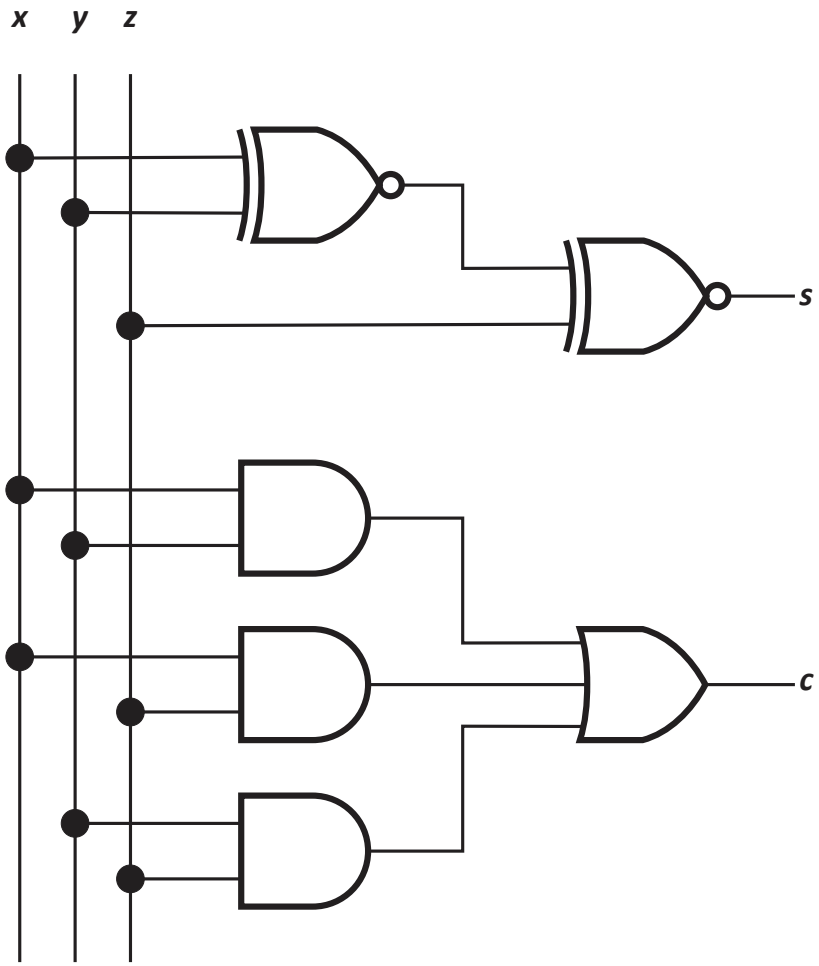
x	y	z	c	s
0	0	0	0	1
0	0	1	0	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	0

d.

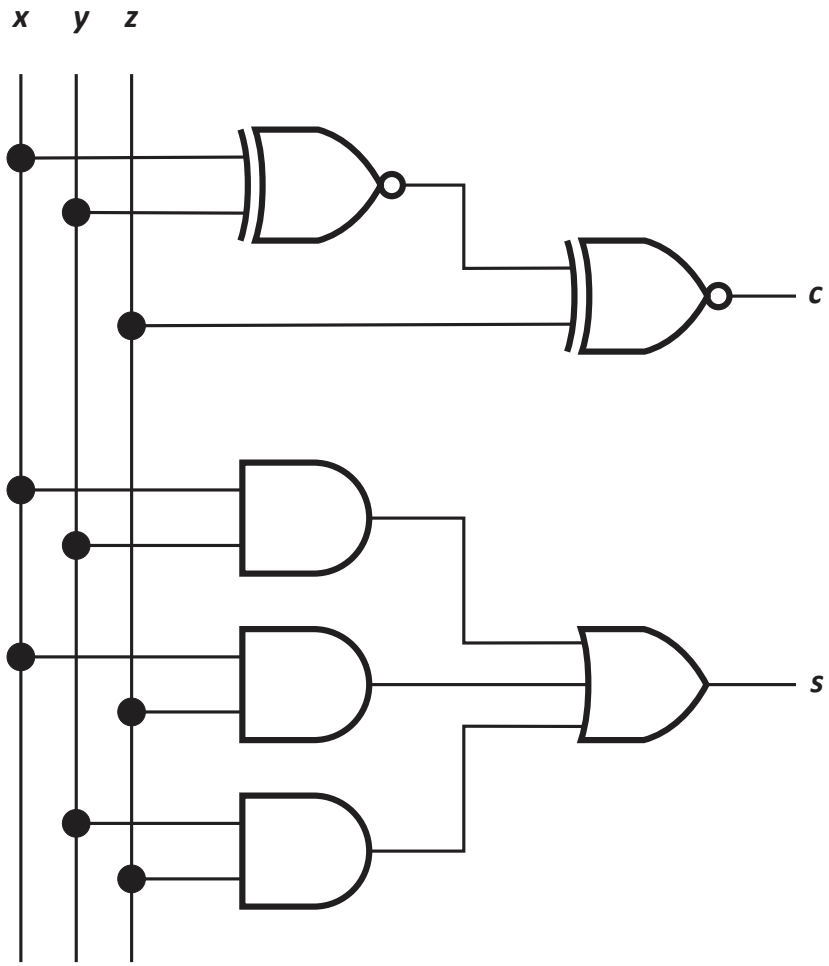
24. Select the logic diagram that implements a full adder.



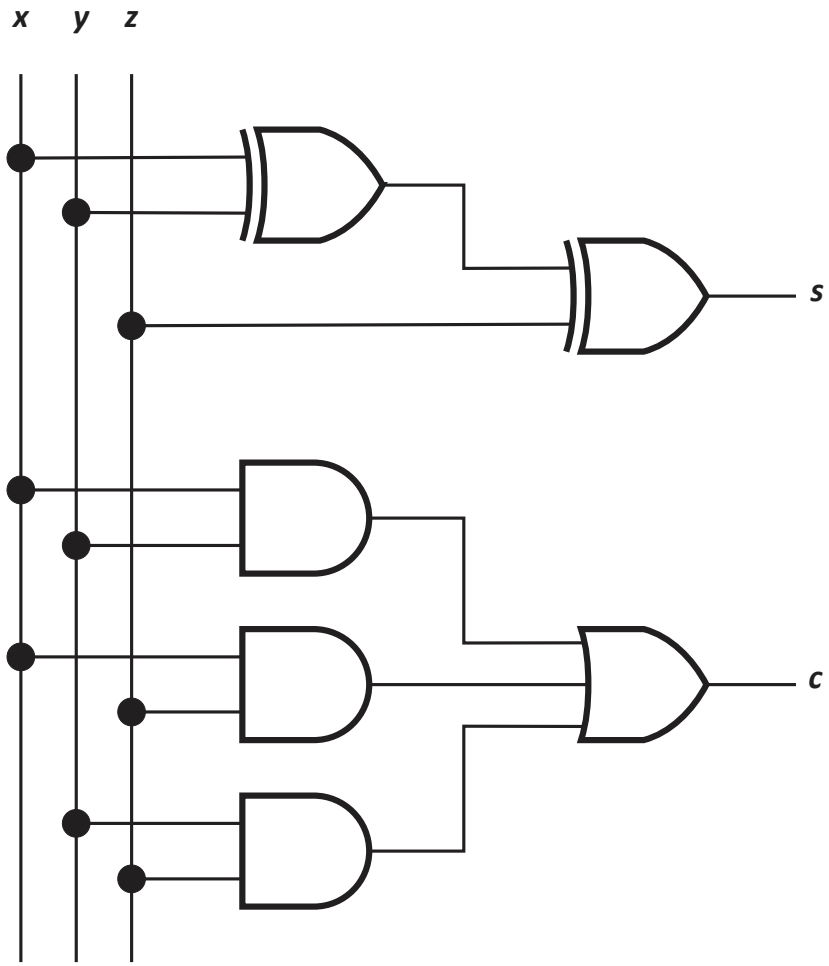
a.



b.



c.



d.

25. Which of the following concerns itself with instruction sets and formats, operation codes, data types, the number and types of registers, addressing modes, main memory access methods, and various I/O mechanisms?

    a. architecture
    b. layers
    c. organization
    d. programming

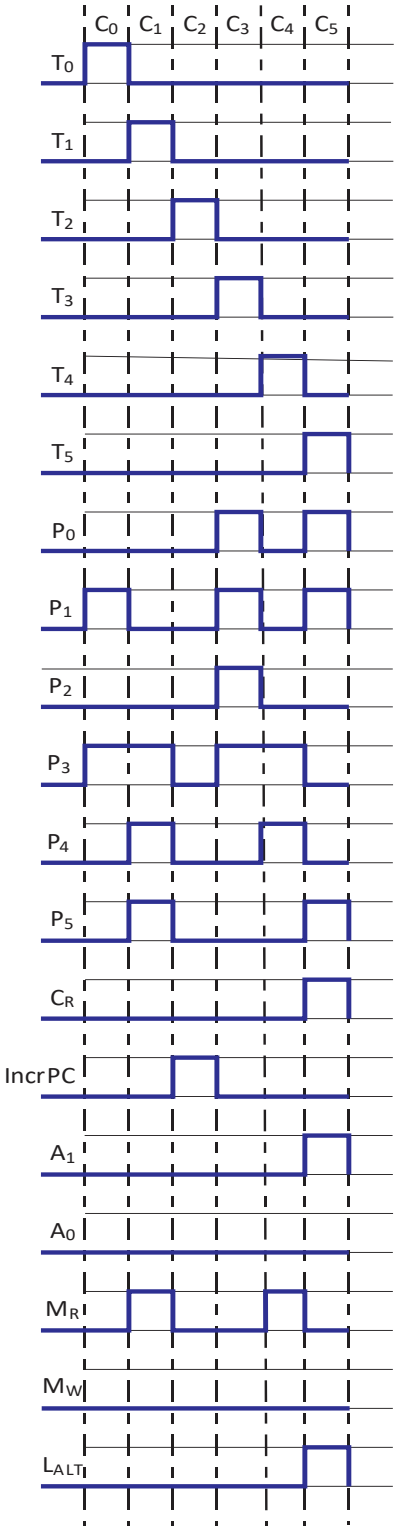


Figure 27. Diagram for Questions 27, 28

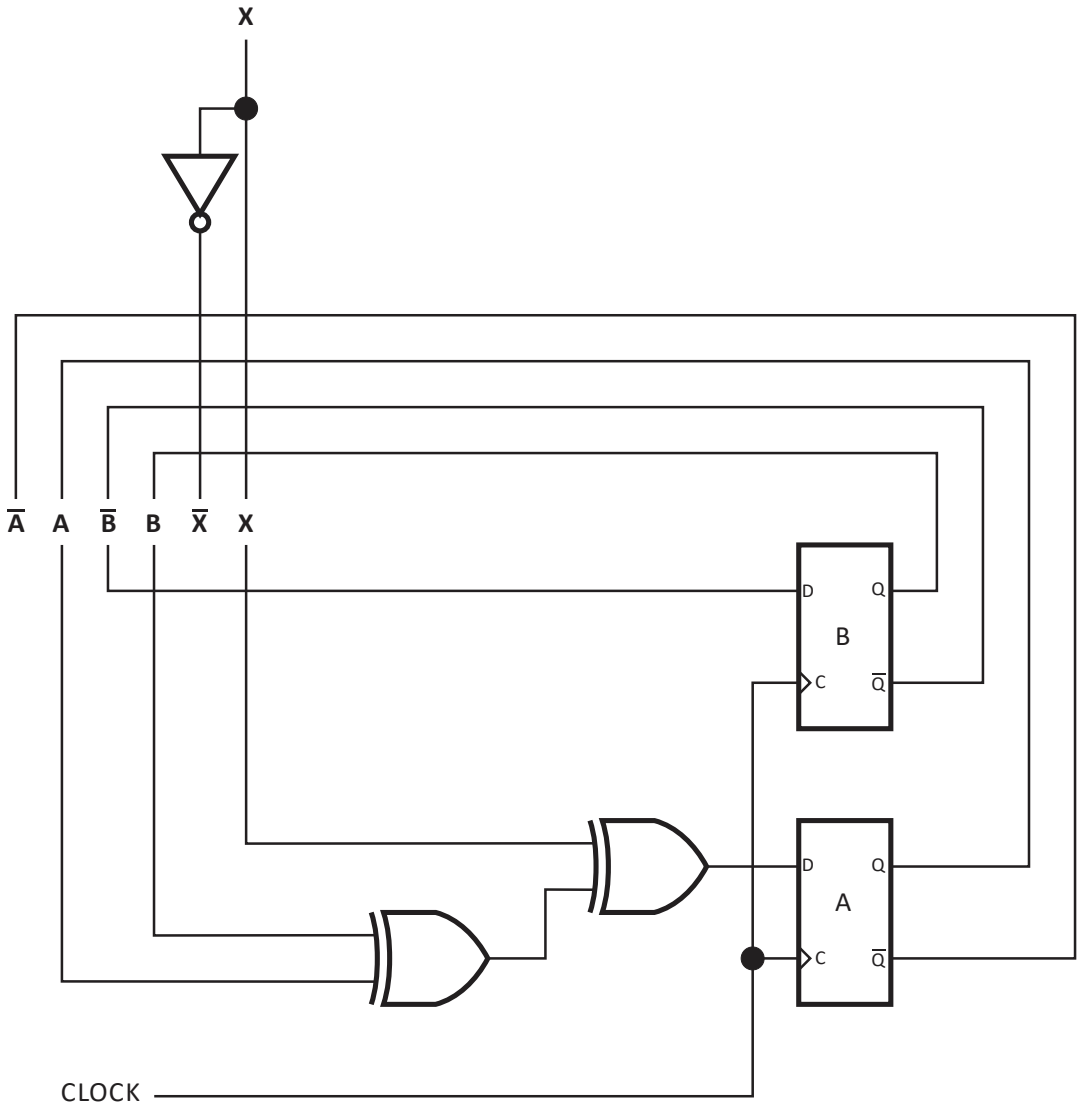
26. Which register transfer is executed at T_3 in the timing diagram of Figure 47?

    a. MAR←PC
    b. IR←M[MAR]
    c. MAR←IR[11-0]
    d. PC←PC+1

27. To which of MARIE's instructions does the timing diagram in Figure 47 refer?

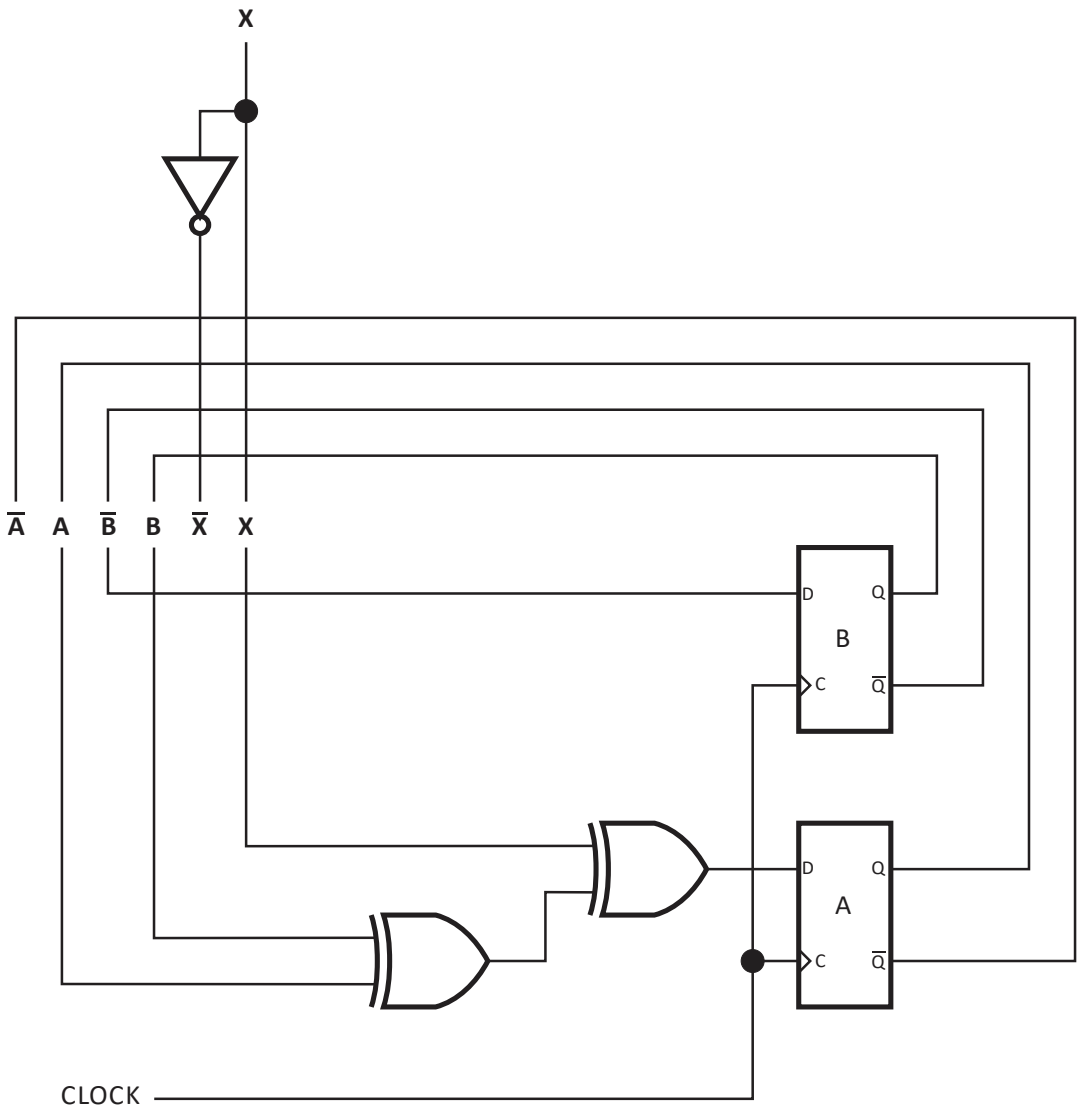
    a. Subt *X*
    b. Load *X*
    c. Store *X*
    d. Add *X*

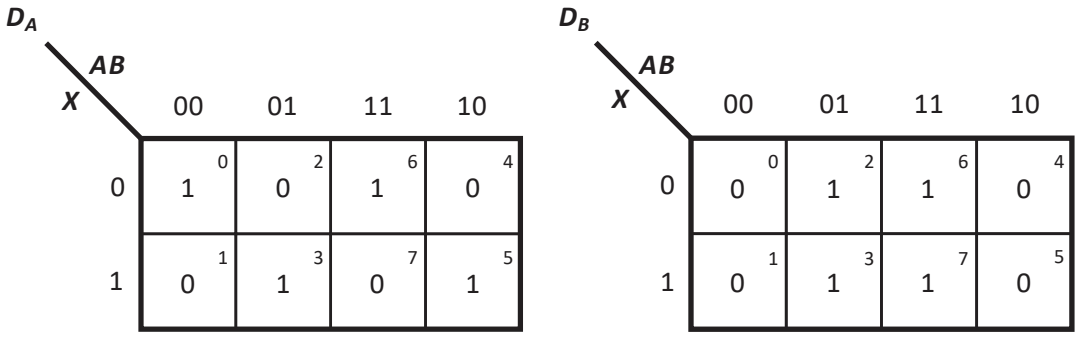
28. Find the equations for the next state decoder in the diagram below.



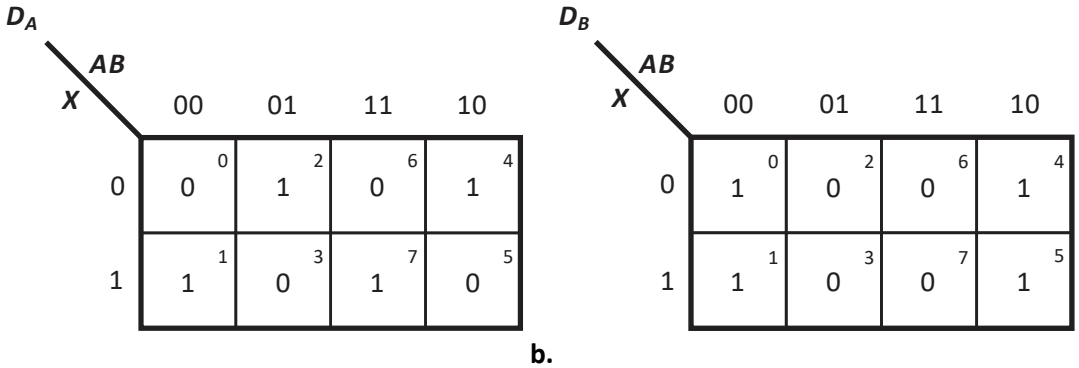
a. $D_A = A + B + X, D_B = \overline{B}$
b. $D_A = A \oplus B \oplus X, D_B = \overline{B}$
c. $D_A = A \oplus B \oplus X, D_B = B$
d. $D_A = A + B + X, D_B = B$

29. Find the K-Maps for the next state decoder in the diagram below.

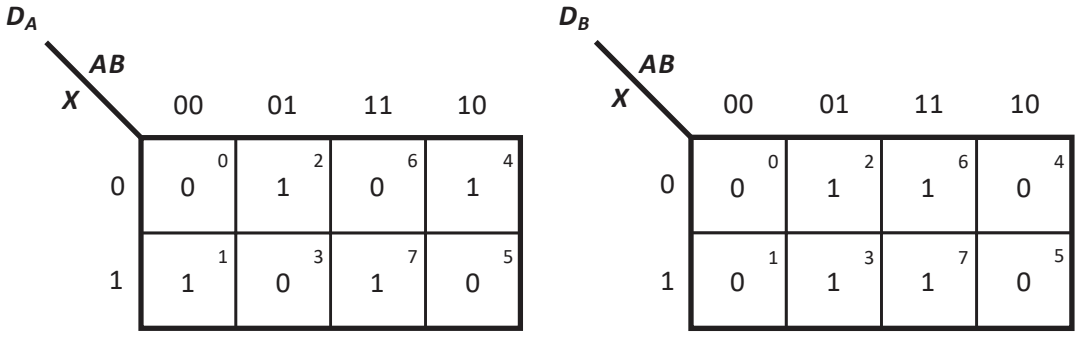



D_A
AB
X
00 01 11 10
0: 1 0 1 0
1: 0 1 0 1
D_B
AB
X
00 01 11 10
0: 0 1 1 0
1: 0 1 1 0

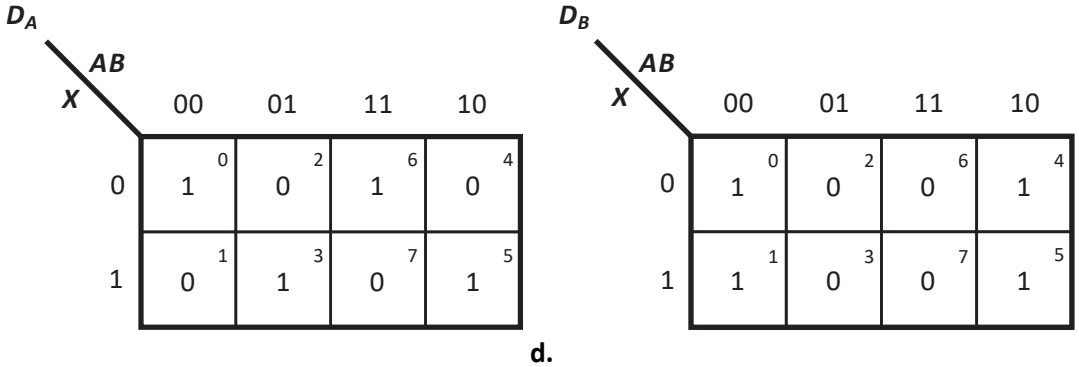
a.


D_A
AB
X
00 01 11 10
0: 0 1 0 1
1: 1 0 1 0
D_B
AB
X
00 01 11 10
0: 1 0 0 1
1: 1 0 0 1

b.

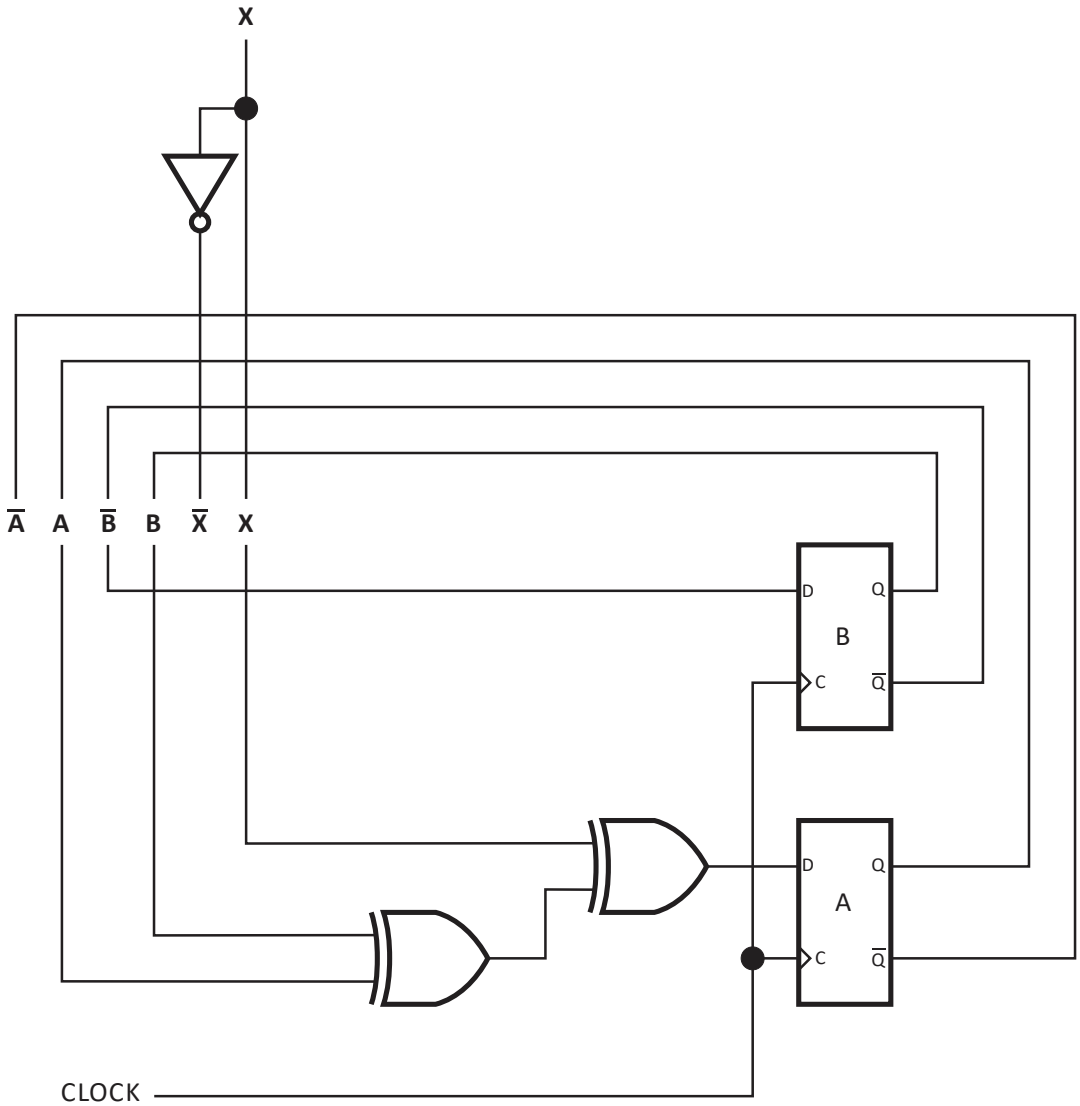

D_A
AB
X
00 01 11 10
0: 0 1 0 1
1: 1 0 1 0
D_B
AB
X
00 01 11 10
0: 0 1 1 0
1: 0 1 1 0

c.


D_A
AB
X
00 01 11 10
0: 1 0 1 0
1: 0 1 0 1
D_B
AB
X
00 01 11 10
0: 1 0 0 1
1: 1 0 0 1

d.

30. Derive the state table for the sequential circuit in the diagram below.



Current State				Next State Decoder			Next State	
A	B	X		D_A	D_B		A	B
0	0	0		1	1		1	1
0	0	1		0	1		0	1
0	1	0		0	0		0	0
0	1	1		1	0		1	0
1	0	0		0	1		0	1
1	0	1		1	1		1	1
1	1	0		1	0		1	0
1	1	1		0	0		0	0

a.

Current State				Next State Decoder			Next State	
A	B	X		D_A	D_B		A	B
0	0	0		1	0		1	0
0	0	1		0	0		0	0
0	1	0		0	1		0	1
0	1	1		1	1		1	1
1	0	0		0	0		0	0
1	0	1		1	0		1	0
1	1	0		1	1		1	1
1	1	1		0	1		0	1

b.

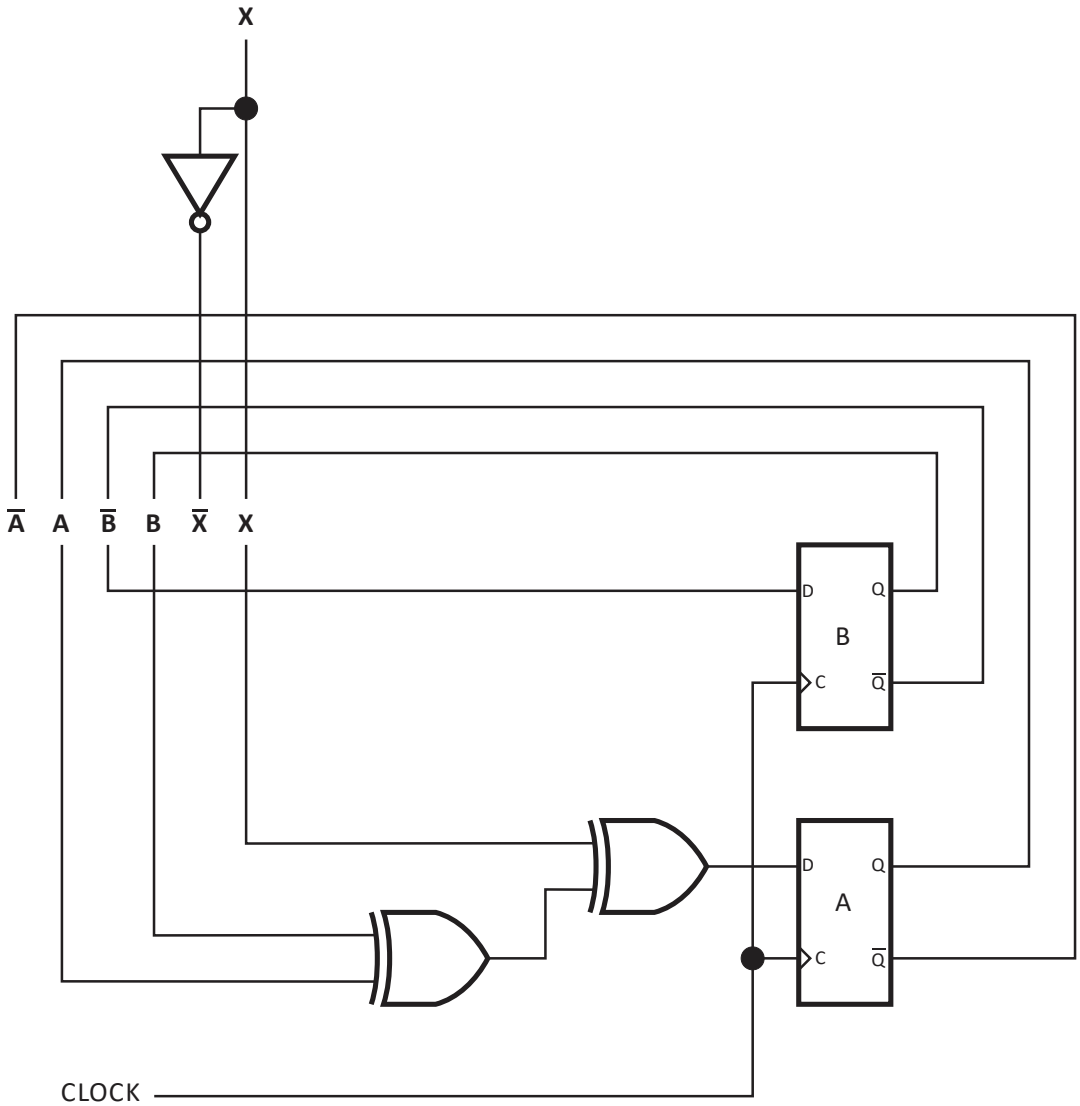
Current State				Next State Decoder			Next State	
A	B	X		D_A	D_B		A	B
0	0	0		0	1		0	1
0	0	1		1	1		1	1
0	1	0		1	0		1	0
0	1	1		0	0		0	0
1	0	0		1	1		1	1
1	0	1		0	1		0	1
1	1	0		0	0		0	0
1	1	1		1	0		1	0

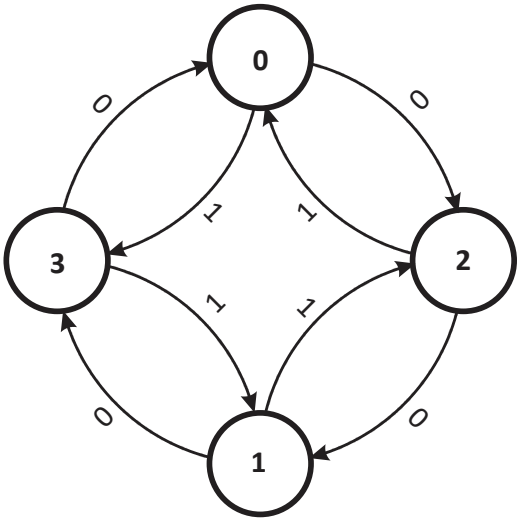
c.

Current State				Next State Decoder			Next State	
A	B	X		D_A	D_B		A	B
0	0	0		0	0		1	0
0	0	1		1	0		0	0
0	1	0		1	1		0	1
0	1	1		0	1		1	1
1	0	0		1	0		0	0
1	0	1		0	0		1	0
1	1	0		0	1		1	1
1	1	1		1	1		0	1

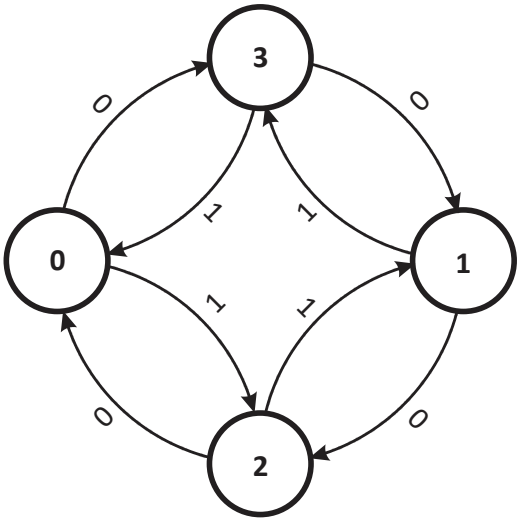
d.

31. Derive the state diagram for the sequential circuit in the diagram below.

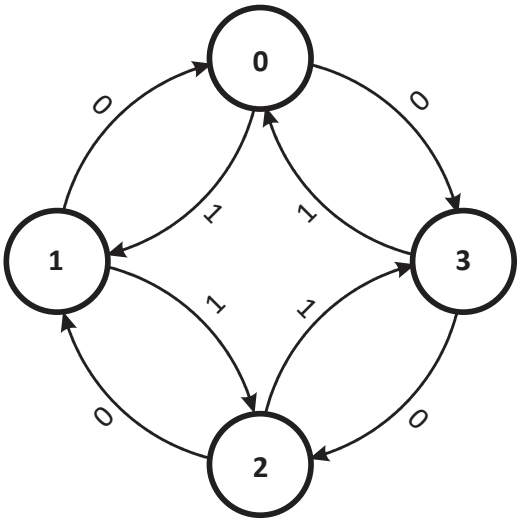




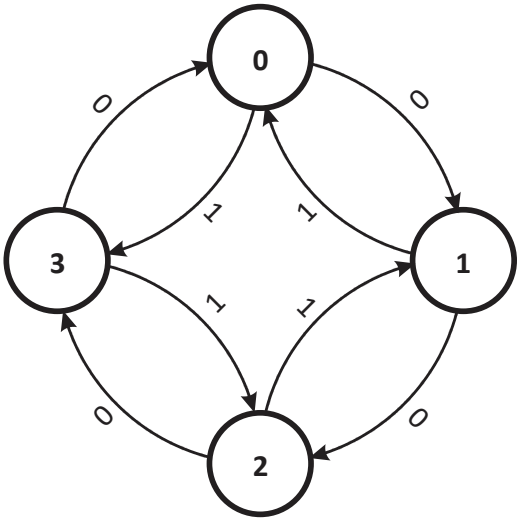
a.



b.

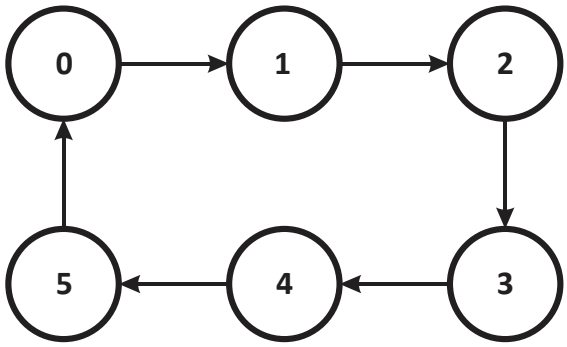


c.



d.

32. Select the state table that corresponds to the state diagram for the sequential circuit in the below.



Current State				Next State				Next State Decoder							
A	B	C		A	B	C		J_A	K_A		J_B	K_B		J_C	K_C
0	0	0		0	0	1		x	x		x	x		1	x
0	0	1		0	1	0		0	x		0	x		x	1
0	1	0		0	1	1		1	x		0	x		1	x
0	1	1		1	0	0		x	0		0	x		x	1
1	0	0		1	0	1		x	1		1	x		1	x
1	0	1		0	0	0		0	x		x	0		x	1
1	1	0		x	x	x		0	x		x	1		x	x
1	1	1		x	x	x		x	x		x	x		x	x

a.

Current State				Next State				Next State Decoder							
A	B	C		A	B	C		J_A	K_A		J_B	K_B		J_C	K_C
0	0	0		x	x	x		x	x		x	x		x	x
0	0	1		0	0	1		0	x		0	x		1	x
0	1	0		0	1	0		0	x		1	x		x	1
0	1	1		0	1	1		0	x		x	0		1	x
1	0	0		1	0	0		1	x		x	1		x	1
1	0	1		1	0	1		x	0		0	x		1	x
1	1	0		0	0	0		x	1		0	x		x	1
1	1	1		x	x	x		x	x		x	x		x	x

b.

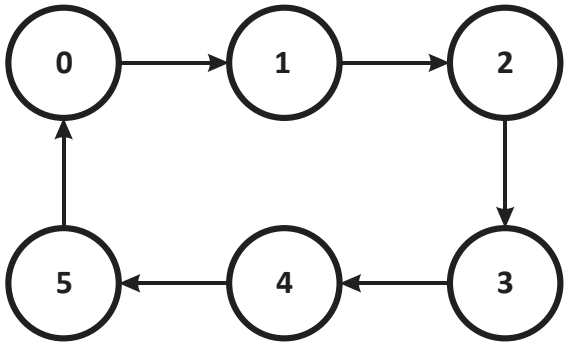
Current State				Next State				Next State Decoder							
A	B	C		A	B	C		J_A	K_A		J_B	K_B		J_C	K_C
0	0	0		0	0	1		0	x		0	x		1	x
0	0	1		0	1	0		0	x		1	x		x	1
0	1	0		0	1	1		0	x		x	0		1	x
0	1	1		1	0	0		1	x		x	1		x	1
1	0	0		1	0	1		x	0		0	x		1	x
1	0	1		0	0	0		x	1		0	x		x	1
1	1	0		x	x	x		x	x		x	x		x	x
1	1	1		x	x	x		x	x		x	x		x	x

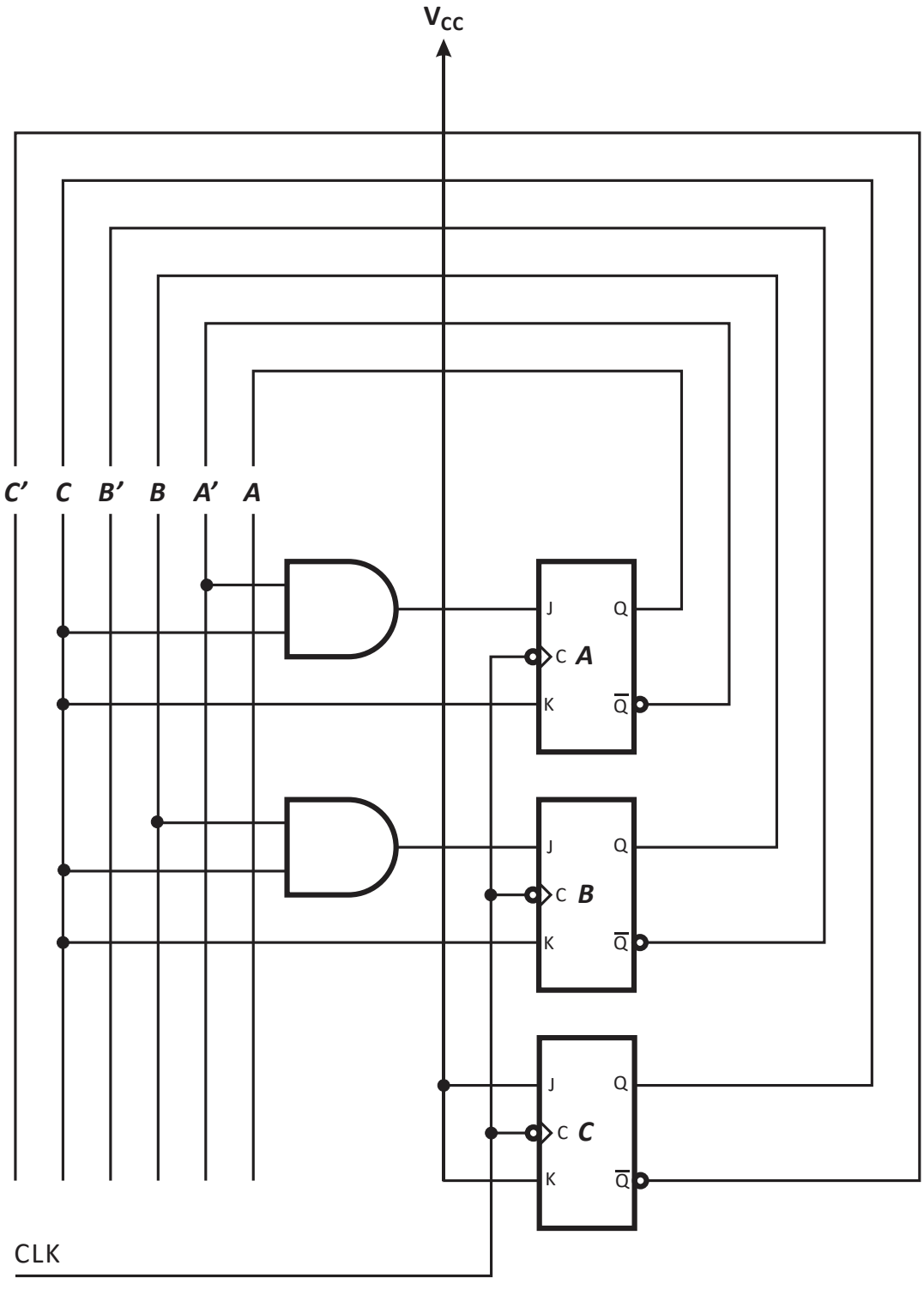
c.

Current State				Next State				Next State Decoder							
A	B	C		A	B	C		J_A	K_A		J_B	K_B		J_C	K_C
0	0	0		x	x	x		x	x		x	x		x	x
0	0	1		x	x	x		x	x		x	x		x	x
0	1	0		0	0	1		0	x		0	x		1	x
0	1	1		0	1	0		0	x		1	x		x	1
1	0	0		0	1	1		0	x		x	0		1	x
1	0	1		1	0	0		1	x		x	1		x	1
1	1	0		1	0	1		x	0		0	x		1	x
1	1	1		0	0	0		x	1		0	x		x	1

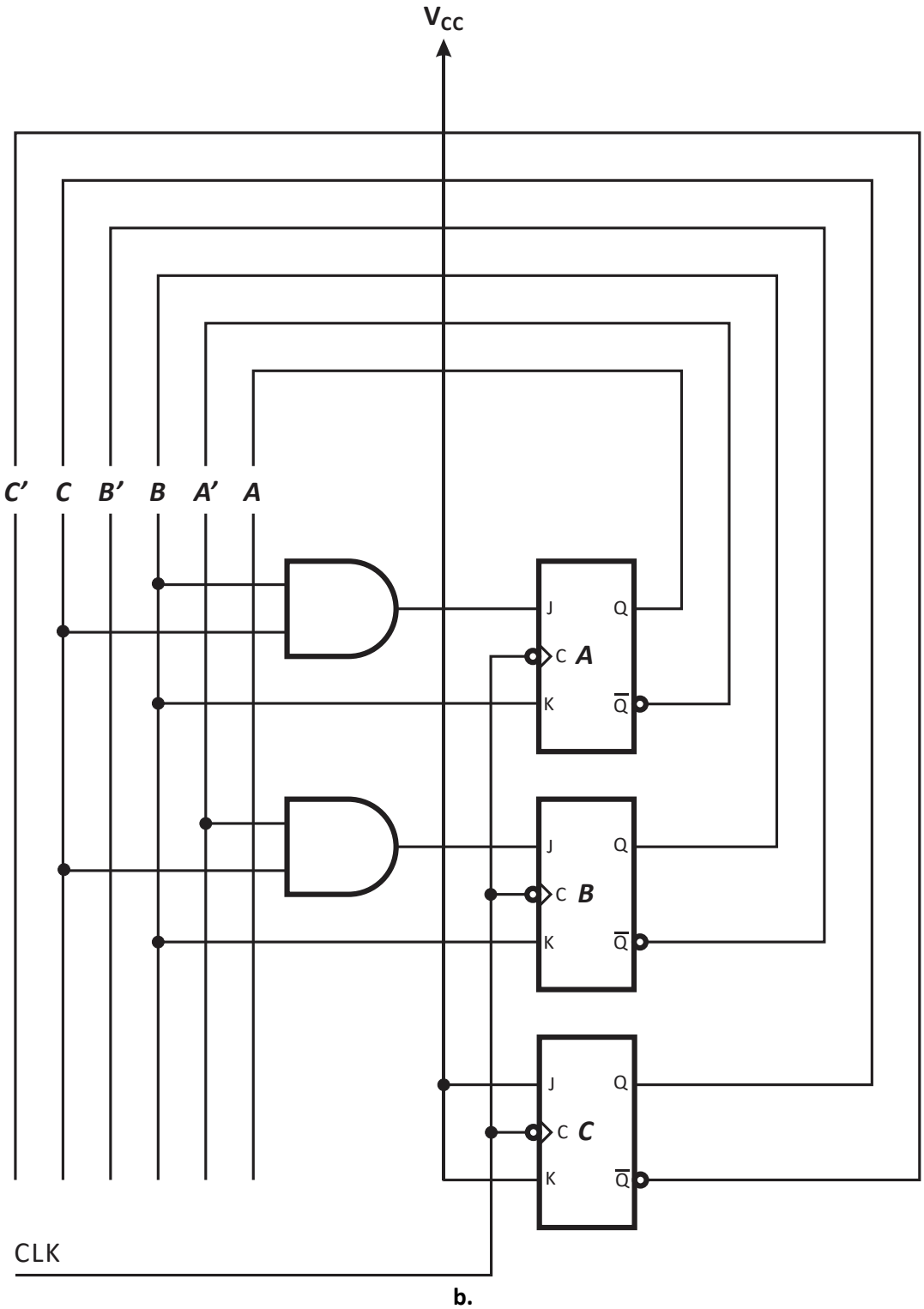
d.

33. Select the logic diagram that corresponds to the state diagram for the sequential circuit in the below.

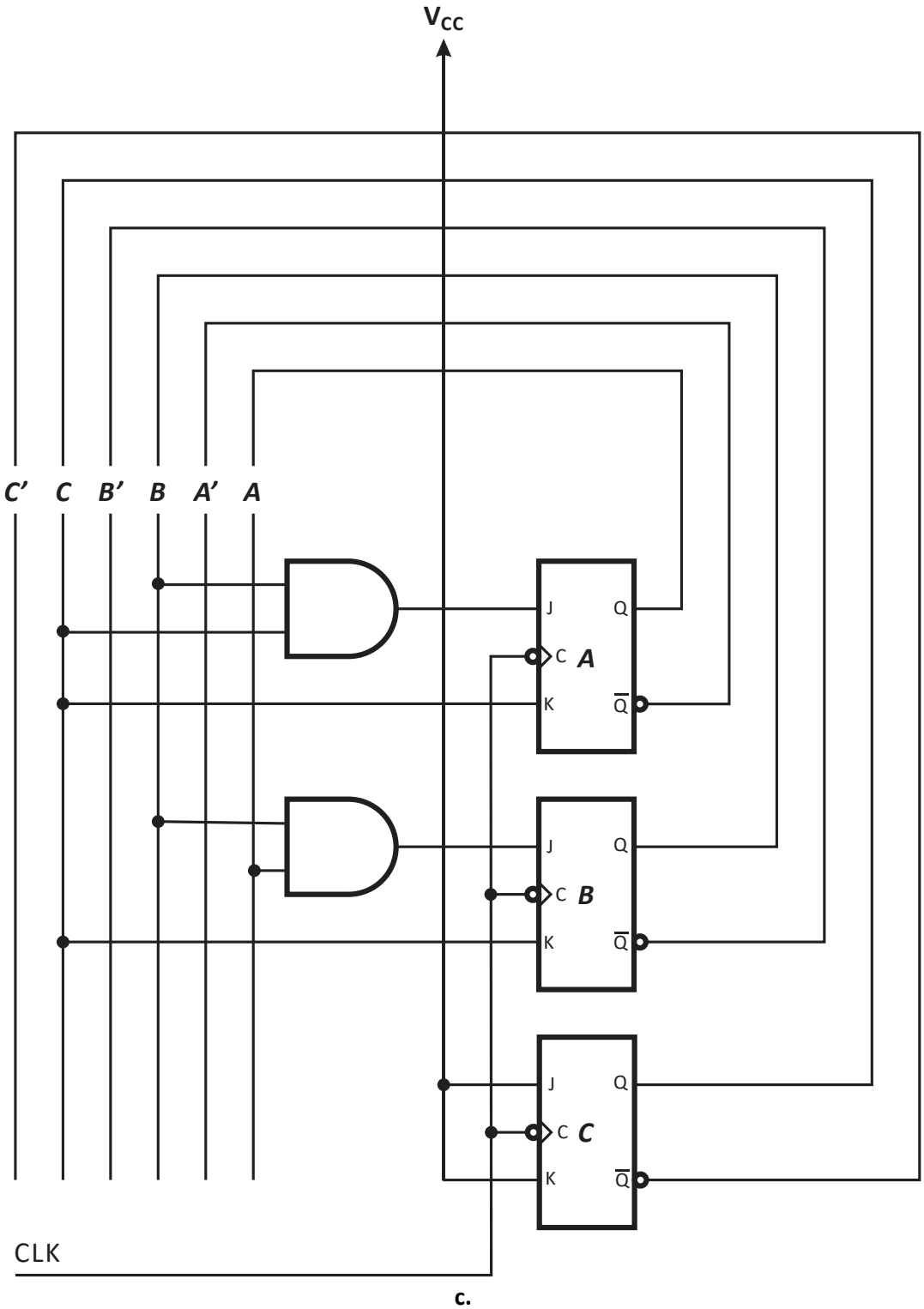



V_{CC}
C' C B' B A' A
J
Q
C A
K
$\overline{Q}$
J
Q
C B
K
$\overline{Q}$
J
Q
C C
K
$\overline{Q}$
CLK

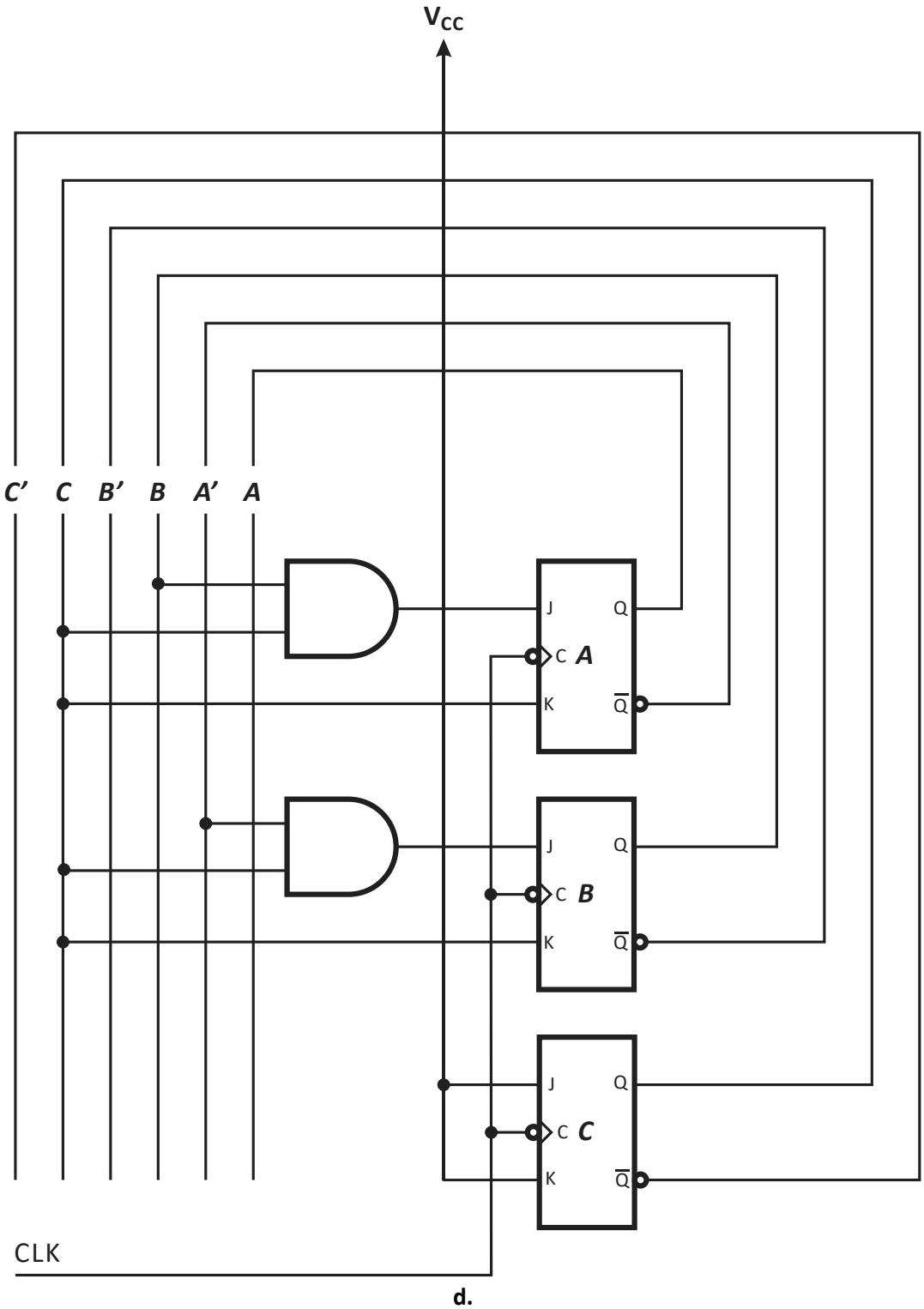
a.


V_{CC}
C' C B' B A' A
J
Q
C A
K
$\overline{Q}$
J
Q
C B
K
$\overline{Q}$
J
Q
C C
K
$\overline{Q}$
CLK

b.


V_{CC}
C' C B' B A' A
J
Q
C A
K
$\overline{Q}$
J
Q
C B
K
$\overline{Q}$
J
Q
C C
K
$\overline{Q}$
CLK

c.


V_{CC}
C' C B' B A' A
J
Q
C A
K
$\overline{Q}$
J
Q
C B
K
$\overline{Q}$
J
Q
C C
K
$\overline{Q}$
CLK

d.

34. Select the characteristic table for a T-Flip-flop that inverts the current state when $T = 1$ and retains the current state when $T = 0$.

T	*Qn*	*Qn+1*
0	0	0
0	1	1
1	0	1
1	1	0

Characteristic Table

a.

T	*Qn*	*Qn+1*
0	0	1
0	1	0
1	0	0
1	1	1

Characteristic Table

b.

Qn	→	*Qn+1*	*T*
0		0	0
0		1	1
1		0	1
1		1	0

Characteristic Table

c.

Qn	→	*Qn+1*	*T*
0		0	1
0		1	0
1		0	0
1		1	1

Characteristic Table

d.

35. Augment the characteristic table for a T-Flip-flop to design the flip-flop from an S-R Flip-Flop.

T	*Qn*	*Qn+1*	S	R
0	0	0	x	0
0	1	1	0	x
1	0	1	0	1
1	1	0	1	0

Augmented Characteristic Table

a.

T	*Qn*	*Qn+1*	S	R
0	0	0	0	x
0	1	1	x	0
1	0	1	1	0
1	1	0	0	1

Augmented Characteristic Table

b.

T	*Qn*	*Qn+1*	S	R
0	0	0	1	0
0	1	1	0	1
1	0	1	0	x
1	1	0	x	0

Augmented Characteristic Table

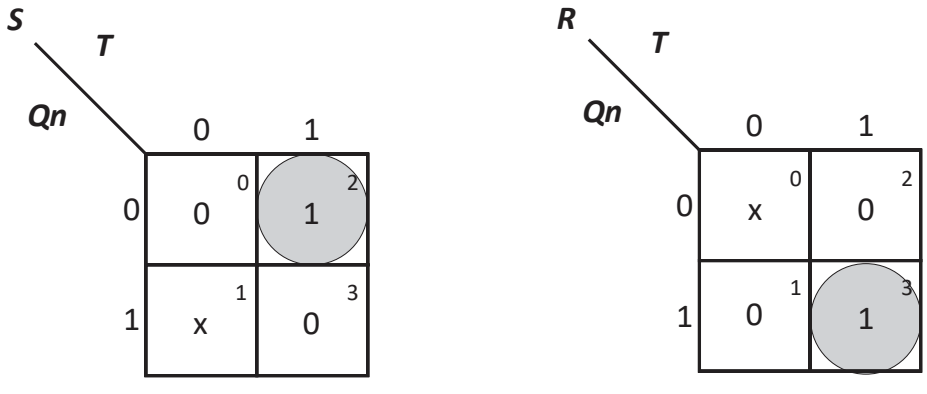
c.

T	*Qn*	*Qn+1*	S	R
0	0	0	0	1
0	1	1	1	0
1	0	1	x	0
1	1	0	0	x

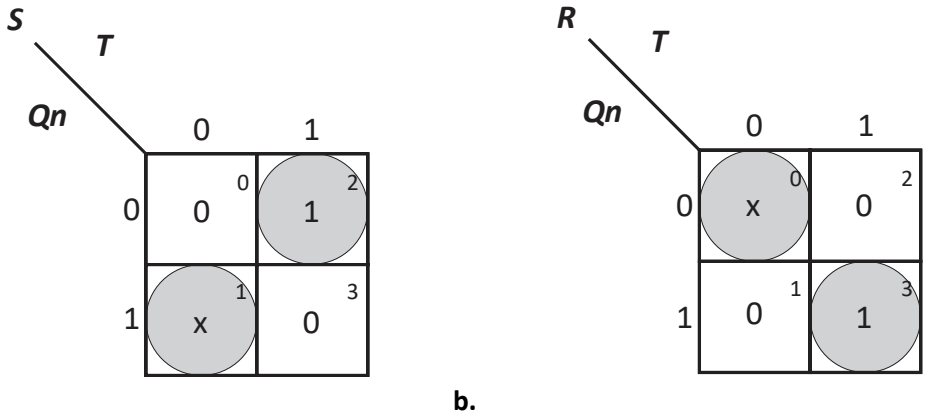
Augmented Characteristic Table

d.

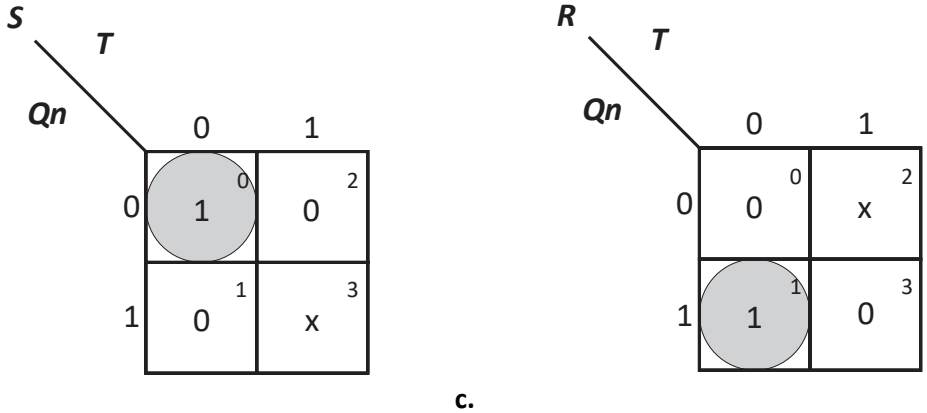
36. Draw K-Maps for the T-Flip-flop.



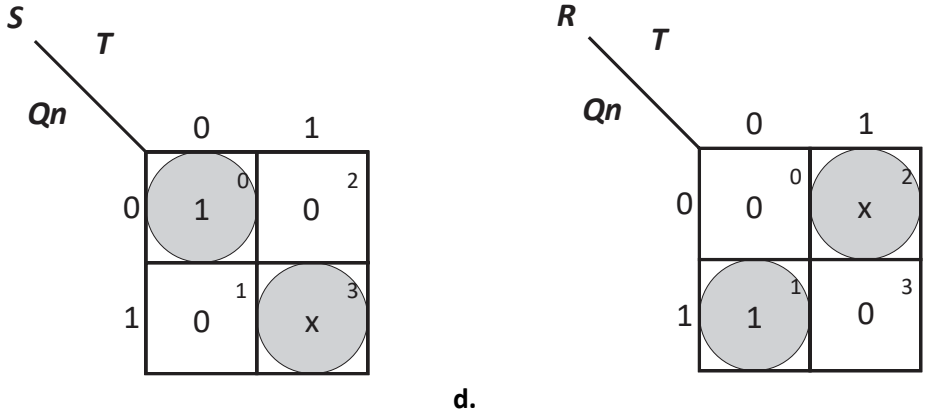
a.



b.

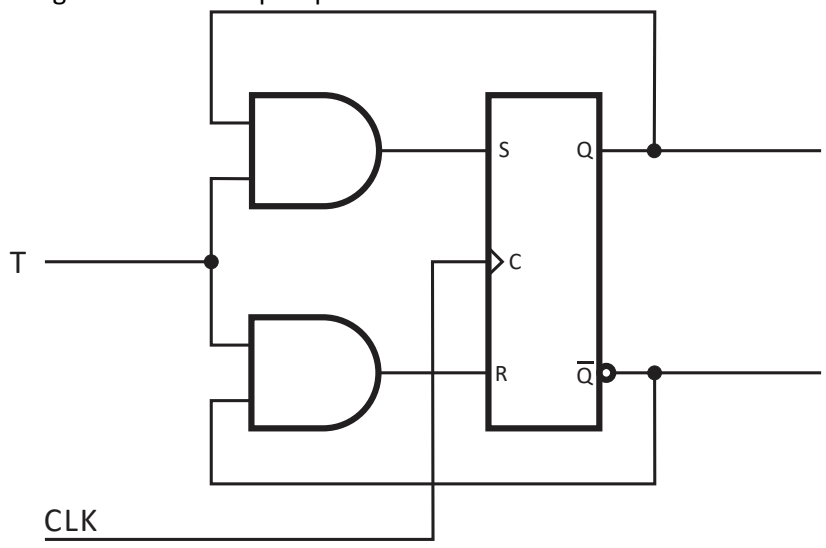


c.

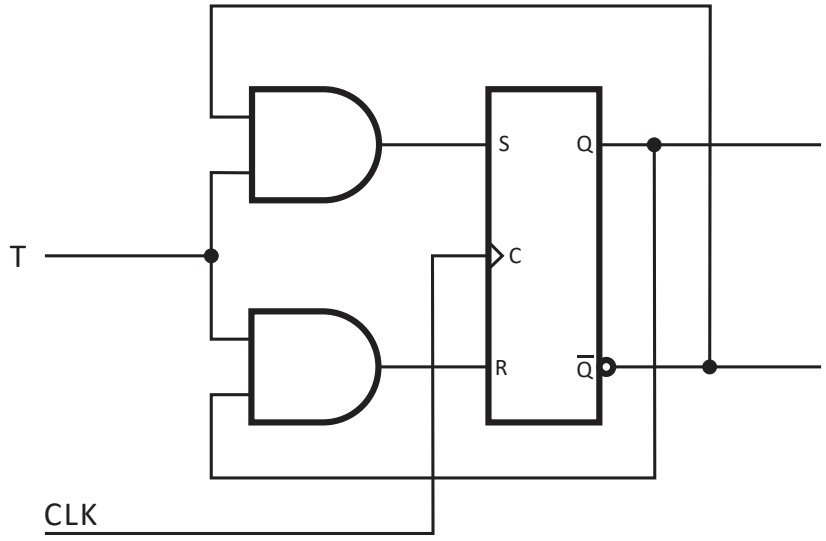


d.

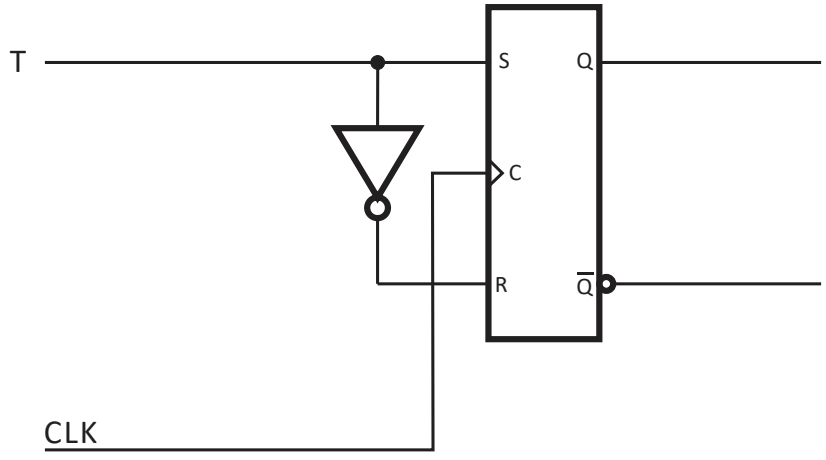
37. Draw a logic diagram for the T-Flip-flop.



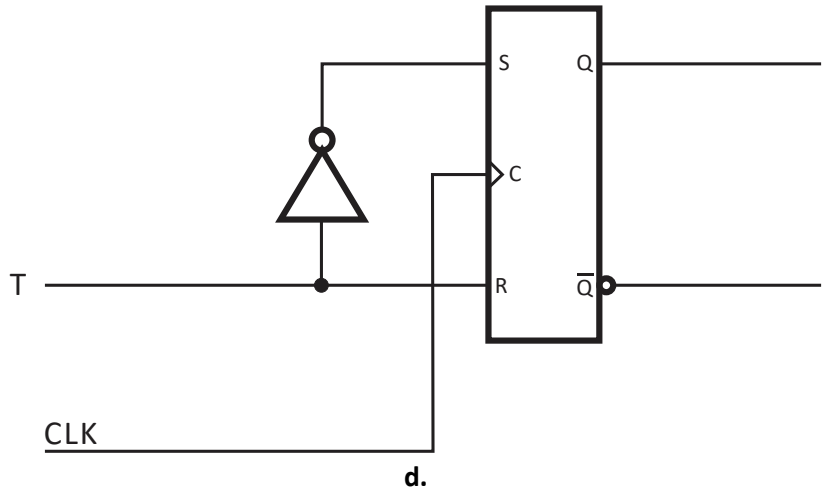
a.



b.



c.



d.

38. A composite memory, 32G × 32 is created using component memory chips, 2G × 8. How many component memory chips are required to create the composite memory?

    a. 2^5
    b. 2^4
    c. 2^6
    d. 2^7

39. A composite memory, 32G × 32 is created using component memory chips, 2G × 8. How many address lines are required to access the composite memory?

    a. 34
    b. 31
    c. 32
    d. 35

40. A composite memory, 32G × 32 is created using component memory chips, 2G × 8. How many address lines are connected to the component chips?

    a. 35
    b. 31
    c. 34
    d. 32

41. A composite memory, 32G × 32 is created using component memory chips, 2G × 8. How many of the address lines must be decoded to produce the chip select inputs?

    a. 5
    b. 6
    c. 3
    d. 4

42. A composite memory, 32G × 32 is created using component memory chips, 2G × 8. How many component memory chips are connected to each output of the decoder?

    a. 5
    b. 6
    c. 4
    d. 3

43. A composite memory, 32G × 32 is created using component memory chips, 2G × 8. Specify the size of the decoder needed to construct the composite memory.

    a. 5-line-to-32-line decoder
    b. 6-line-to-64-line decoder
    c. 3-line-to-8-line decoder
    d. 4-line-to-16-line decoder

44. How many address lines are required to address a 1M × 8 main memory if the memory is byte-addressable?

    a. 19 address lines
    b. 20 address lines
    c. 18 address lines
    d. 17 address lines

45. How many address lines are required to address a 1M × 8 main memory if the memory is word-addressable and each word consists of 8 bytes?

    a. 17 address lines
    b. 20 address lines
    c. 19 address lines
    d. 18 address lines

46. Select the correct Register Transfer Notation (RTN) sequence for the MARIE Store instruction.

a.

MAR	**←**	**PC**
IR	**←**	**M[MAR}**
PC	**←**	**PC+1**
MAR	**←**	**X**
MBR	**←**	**M[MAR]**
PC	**←**	**MBR**

b.

MAR	**←**	**PC**
IR	**←**	**M[MAR}**
PC	**←**	**PC+1**
MAR	**←**	**X**
MBR	**←**	**AC**
M[MAR]	**←**	**MBR**

MAR	←	**PC**
IR	←	**M[MAR}**
PC	←	**PC+1**
MAR	←	**X**
MBR	←	**M[MAR]**
AC	←	**MBR**

c.

MAR	←	**PC**
IR	←	**M[MAR}**
PC	←	**PC+1**
MAR	←	**X**
MBR	←	**M[MAR]**
AC	←	**AC+MBR**

d.

47. Select the correct signal pattern for the register transfer **MAR**← $\boldsymbol{X}$ during clock signal T_3. The table of control signals and their associated registers is given to assist you for this question.

Register	**Memory**	**MAR**	**PC**	**MBR**	**AC**	**IN**	**OUT**	**IR**
Signals								
$P_2P_1P_0$ (Read) **$P_5P_4P_3$(Write)**	000	001	010	011	100	101	110	111

a. $\mathrm{P_4P_3T_3M_r}$
b. $\mathrm{C_rA_0P_5T_3L_{ALT}}$
c. $\mathrm{P_3P_1T_3}$
d. $\mathrm{P_3P_2P_1P_0T_3}$

48. Among other things, assembler directives can:

a. distinguish a value as hexadecimal or decimal
b. determine the next action after numeric overflow
c. invoke interrupt service routines
d. control conditional assembly using macro instructions

49. What unit is typically used to measure the speed of a computer clock?

a. gigahertz
b. kilohertz
c. megahertz
d. terahertz

50. Find the excess binary representation of -333 in a 12-bit integer field.

a. 0110 1011 0010
b. 0001 0100 1101
c. 1110 1011 0010
d. 1110 1011 0011