- The normal execution of a program is altered when an event of higher-priority occurs. The CPU is alerted to such an event through an interrupt.
- Interrupts can be triggered by I/O requests, arithmetic errors (such as division by zero), or when an invalid instruction is encountered.
- Each interrupt is associated with a procedure that directs the actions of the CPU when an interrupt occurs.
  - Nonmaskable interrupts are high-priority interrupts that cannot be ignored.
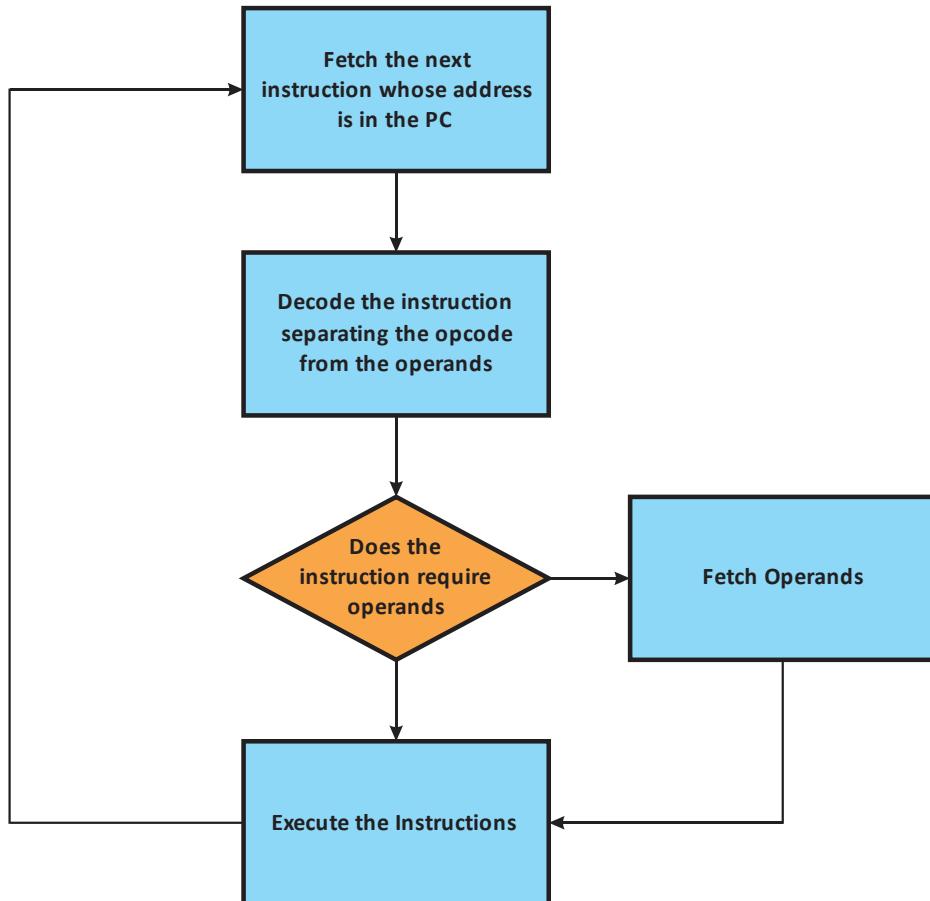
Figure 4.11 The Fetch-Decode-Execute Cycle

```
                    Has an
         Yes     interrupt been     No
                   issued?

  Process the                    Perform the
  interrupt                      fetch-decode-execute
                                 cycle
```
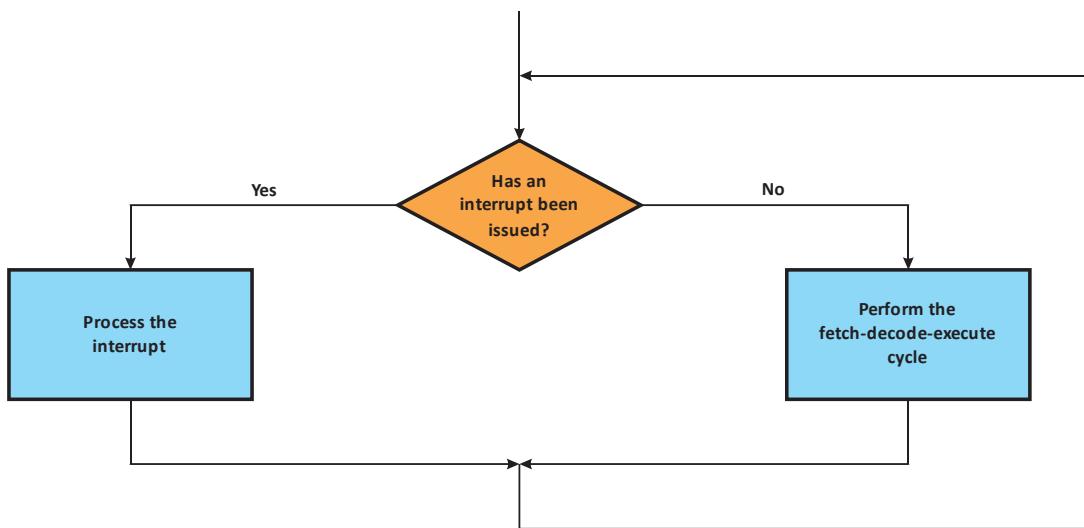
Figure 4.12 The Fetch-Decode-Execute Cycle with Interrupt Checking

```
                    ┌──────────────┐
                    │    Start     │
                    └──────────────┘
                           │
                           ▼
                    ┌──────────────┐
                    │  Interrupt   │
                    │   Signal     │
                    │  Detected    │
                    └──────────────┘
                           │
                           ▼
                    ┌──────────────┐
                    │    Save      │
                    │ variables and│
                    │  registers   │
                    └──────────────┘
                           │
                           ▼
                    ┌──────────────┐
                    │ Look up ISR  │
                    │ address in   │
                    │interrupt vector
                    │    table     │
                    └──────────────┘
                           │
                           ▼
                    ┌──────────────┐
                    │  Place ISR   │
                    │   address    │
                    │    in PC     │
                    └──────────────┘
                           │
                           ▼
                    ┌──────────────┐        ┌──────────────┐
                    │ Branch to ISR│──────▶ │    Start     │
                    └──────────────┘        └──────────────┘
                                                    │
                                                    ▼
                                            ┌──────────────┐
                                            │ Perform work │
                                            │ specific to  │
                                            │  interrupt   │
                                            └──────────────┘
                                                    │
                                                    ▼
                    ┌──────────────┐        ┌──────────────┐
                    │   Restore    │◀────── │    Return    │
                    │saved variables│       └──────────────┘
                    │ and registers│
                    └──────────────┘
                           │
                           ▼
                    ┌──────────────┐
                    │Branch to top of
                    │fetch-decode-execute
                    │    cycle     │
                    └──────────────┘
```
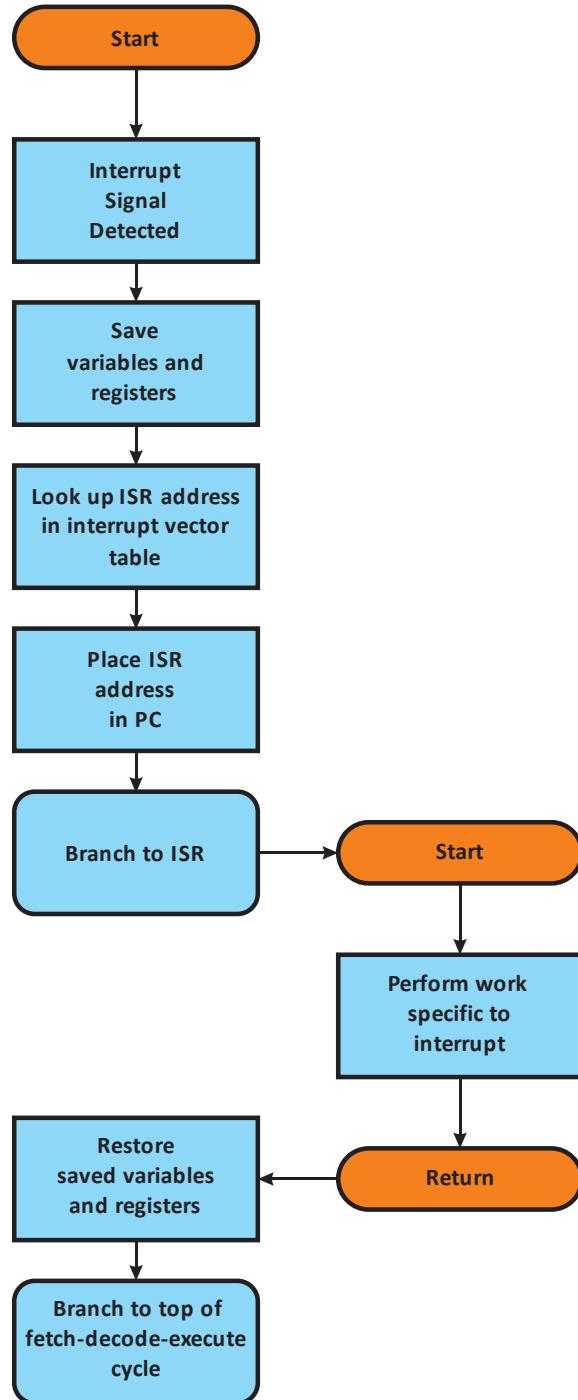
Figure 4.13 Processing and Interrupt