4.6 Memory Organization and Addressing

- Computer memory consists of a linear array of addressable storage cells that are similar to registers.
- Memory can be byte-addressable, or word-addressable, where a word typically consists of two or more bytes.
- Memory is constructed of RAM chips, often referred to in terms of *length* × *width*.
- If the memory word size of the machine is 16 bits, then a 4M × 16 RAM chip gives us 4 megawords of 16-bit memory locations
- How does the computer access a memory location corresponds to a particular address?
- We observe that 4M can be expressed as $2^2 \times 2^{20} = 2^{22}$ words.
- The memory locations for this memory are numbered 0 through $2^{22}-1$.
- Thus, the memory bus of this system requires at least 22 address lines.
  - The address lines "count" from 0 to $2^{22} - 1$ in binary. Each line is either "on" or "off" indicating the location of the desired memory element.
- Physical memory usually consists of more than one RAM chip.
- Access is more efficient when memory is organized into banks of chips with the addresses interleaved across the chips
- With low-order interleaving, the low order bits of the address specify which memory bank contains the address of interest.
- Accordingly, in high-order interleaving, the high order address bits specify the memory bank.

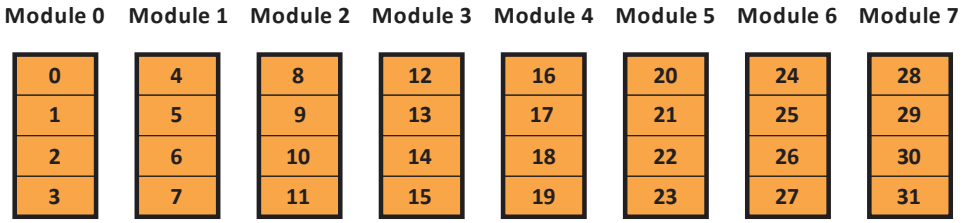


Figure 4.6 (a) High-Order Interleaving

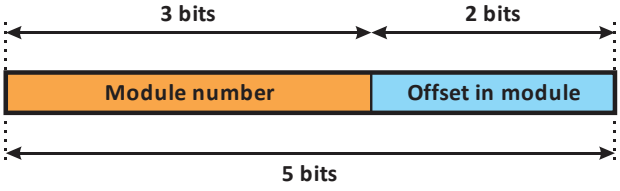


Figure 4.6 (b) Address Structure

Module	Decimal Word Address	Binary Address	Address Split per Given Structure	Module Number	Offset in Module
Module 0	0	00000	000 00	0	0
	1	00001	000 01	0	1
	2	00010	000 10	0	2
	3	00011	000 11	0	3
Module 1	4	00100	001 00	1	0
	5	00101	001 01	1	1
	6	00110	001 10	1	2
	7	00111	001 11	1	3

Figure 4.6 (c) First Two Modules

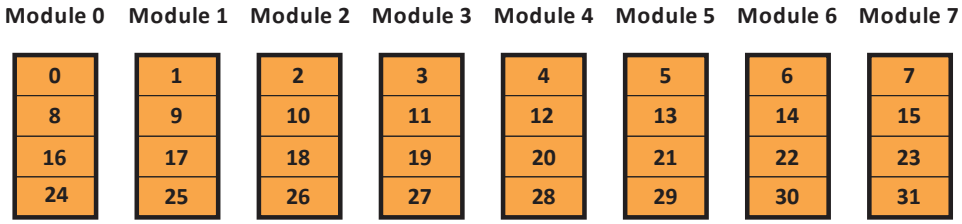


Figure 4.7 (a) Low-Order Interleaving

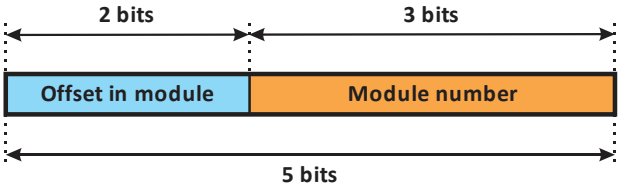


Figure 4.7 (b) Address Structure

Module	Decimal Word Address	Binary Address	Address Split per Given Structure	Module Number	Offset in Module
Module 0	0	00000	00 000	0	0
	8	01000	01 000	1	0
	16	10000	10 000	2	0
	24	11000	11 000	3	0
Module 1	1	00001	00 001	0	1
	9	01001	01 001	1	1
	17	10001	10 001	2	1
	25	11001	11 001	3	1

Figure 4.7 (c) First Two Modules

- Example: Suppose we have a memory consisting of 16 2K x 8 bit chips.
  - Memory is 32K = $2^5 \times 2^{10} = 2^{15}$
  - 15 bits are needed for each address.
  - We need 4 bits to select the chip, and 11 bits for the offset into the chip that selects the byte.

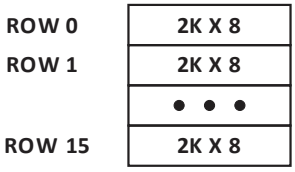
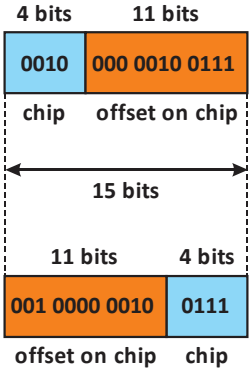
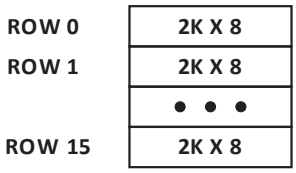
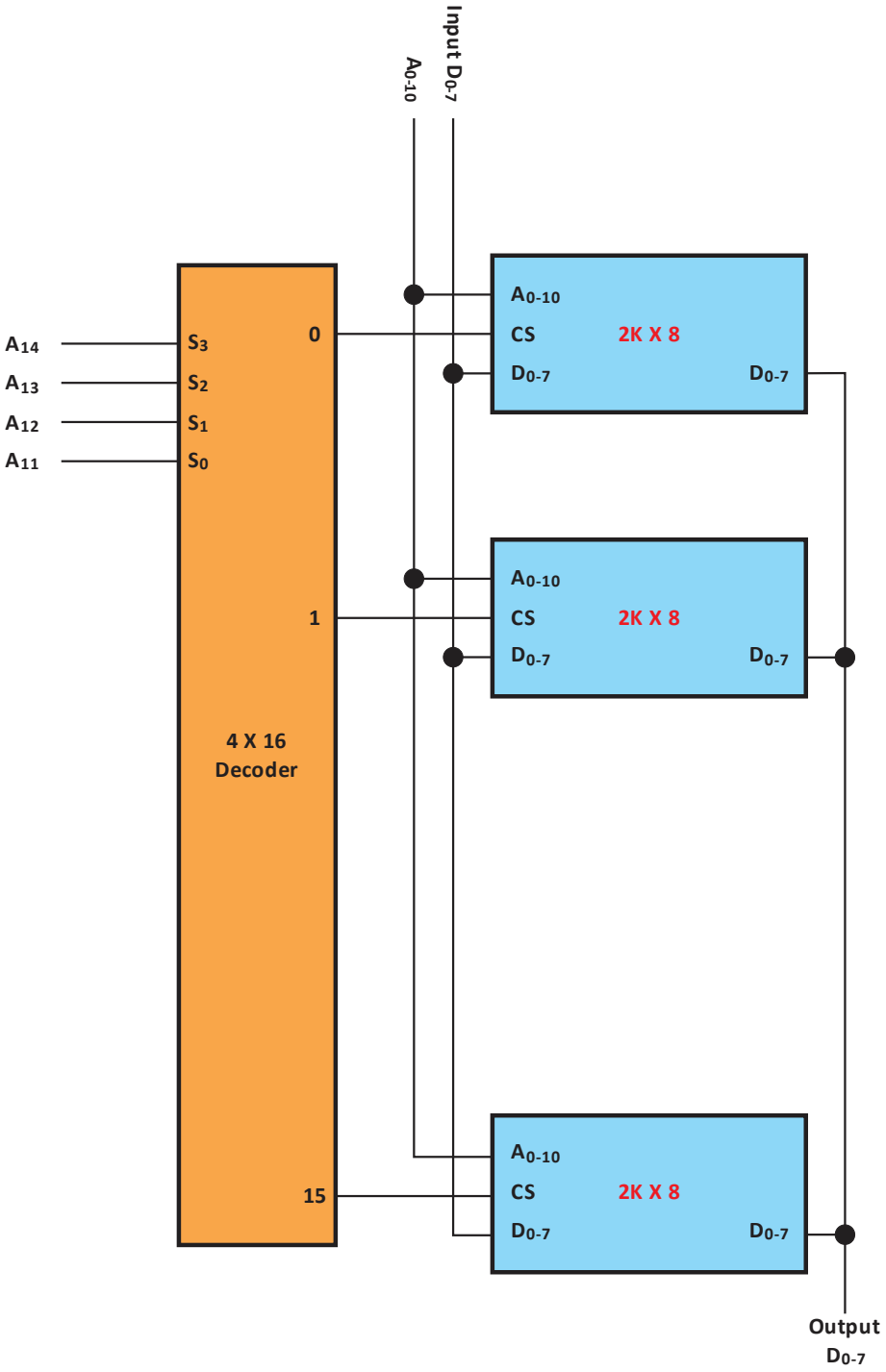


Figure 4.5 Memory as a Collection of RAM Chips

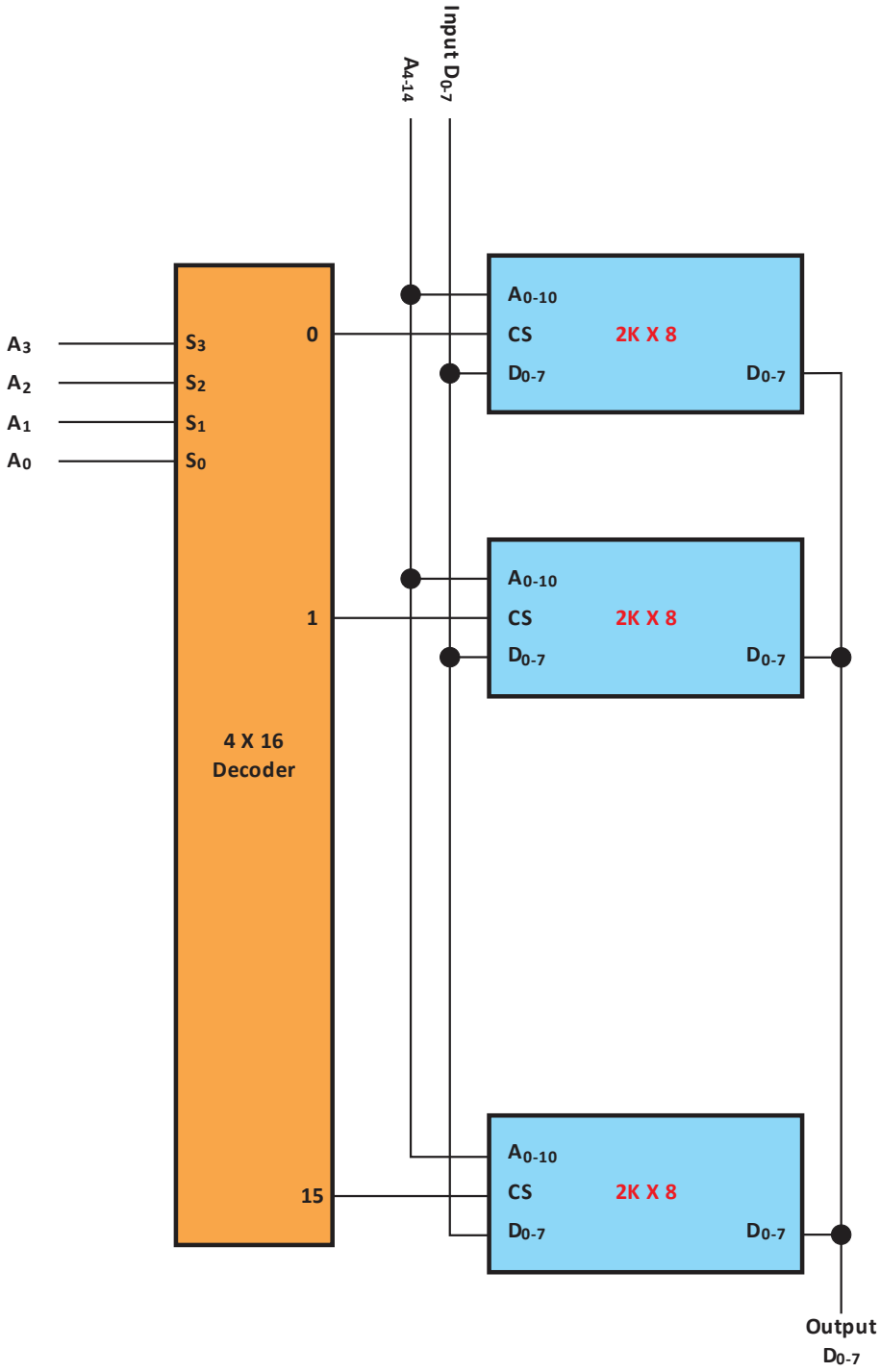
- In high-order interleaving the high-order 4 bits select the chip.
- In low-order interleaving the low-order 4 bits select the chip.







32K Memory constructed with 16 2K X 8 Chips
High-Order Interleaving



32K Memory constructed with 16 2K X 8 Chips
Low-Order Interleaving

10. Suppose that a 2M×16 main memory is built using $256K \times 8$ RAM chips and memory is word addressable.

a) How many RAM chips are necessary?

Solution:

Divide the number of bits in the composite memory by the number of bits in the component chips.

1. **Find the number of bits in the composite memory.**

$$b_T = 2M \times 16 = 2 \times 2^{20} \times 2^4 = 2^{25} bits$$

2. **Find the number of bits in the component memory.**

$$b_C = 256K \times 8 = 2^8 \times 2^{10} \times 2^3 = 2^{21} bits$$

3. **Find the number of RAM chips in the composite memory.**

$$N = \frac{2^{25}}{2^{21}} = 2^4 = 16$$

b) If we were addressing one full word, how many chips would be involved?

Solution:

Divide the number of bits at each address in the composite memory by the number of bits at each address in the component memory chips.

$$n = \frac{16}{8} = 2$$

c) How many address lines are needed for each RAM chip?

Solution:

Find the $\log_2 M$, where M is the number of address cells in the component RAM chips.

$$A = \log_2 256K = \log_2(2^8 \times 2^{10}) = \log_2 2^{18} = 18$$

d) How many banks will this memory have?

Solution:

The number of banks is equal to the number of component chips divided by the number of chips required to access a full word at a single address.

$$K = \frac{16}{2} = 8$$

e) How many address lines are needed for the composite memory?

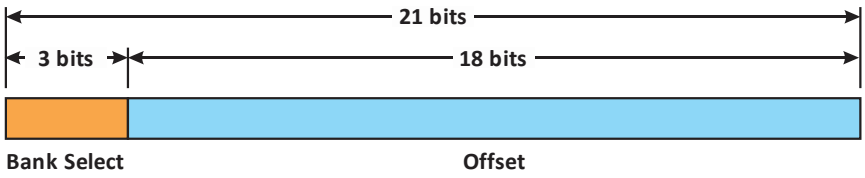
Solution:

Find the $\log_2 M$, where M is the number of address cells in the composite memory.

$$A = \log_2 2M = \log_2(2 \times 2^{20}) = \log_2 2^{21} = 21$$

f) If high-order interleaving is used, where would address 14 (which is E in hex) be located?

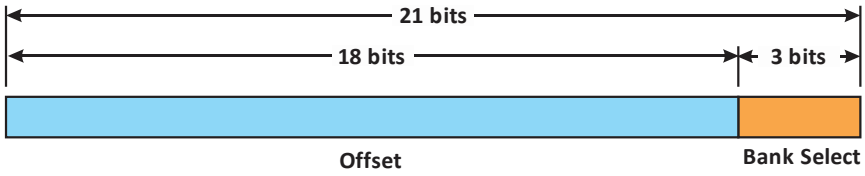
Solution:



Address 14 = 00000E
Bank select is 000

g) Repeat exercise 10f for low-order interleaving.

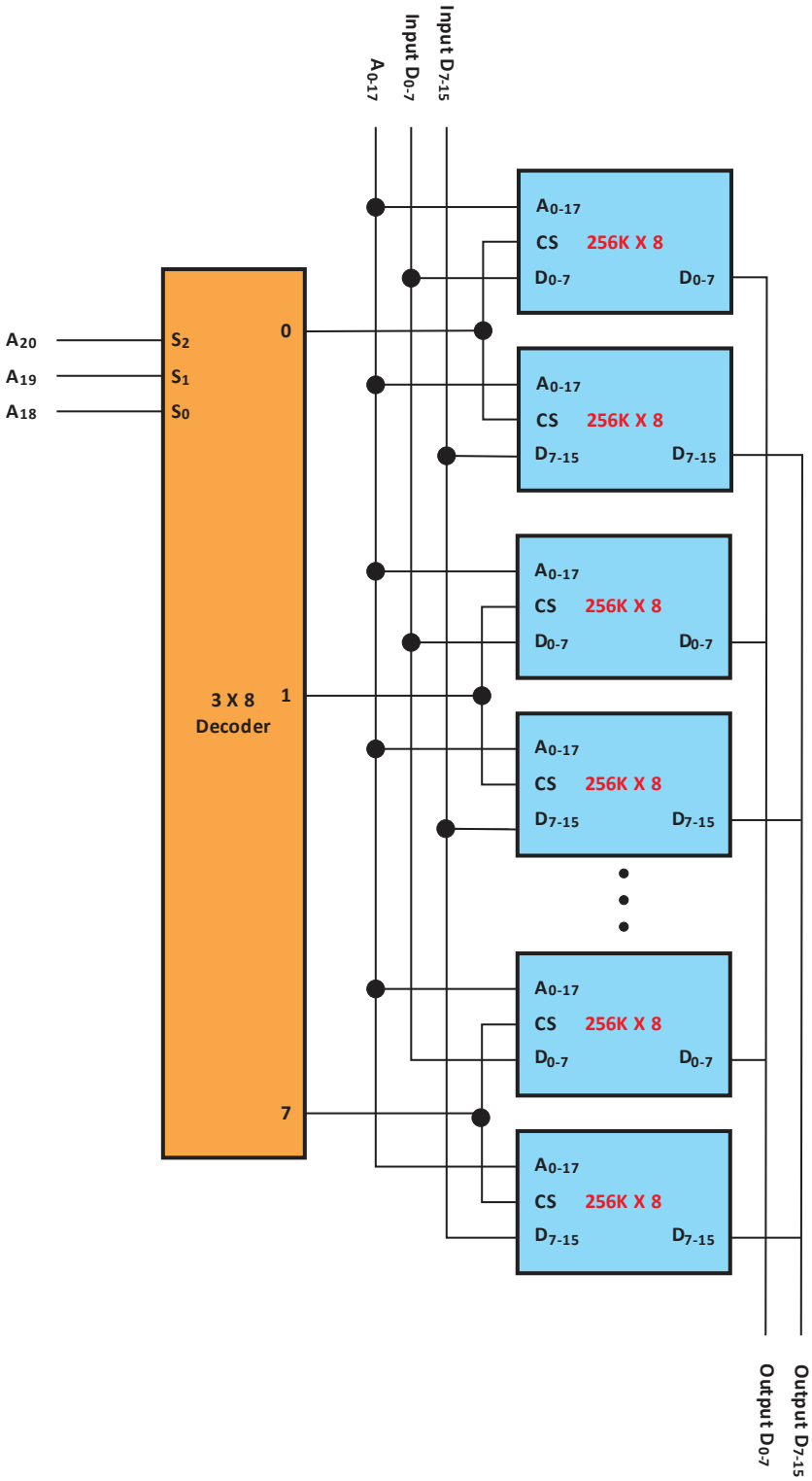
Solution:



Address 14 = 00000E
Bank select is 110=6

h) Draw a logic diagram of the memory that includes a decoder.

Solution:



2M X 16 Memory made from 256K X 8 chips
High-Order Interleaving

Suppose that a $4M \times 32$ main memory is built using $128K \times 8$ RAM chips and memory is word addressable.

a) How many RAM chips are necessary?

Solution:

Divide the number of bits in the composite memory by the number of bits in the component chips.

1. **Find the number of bits in the composite memory.**

$$b_T = 4M \times 32 = 4 \times 2^{20} \times 2^5 = 2^{27} bits$$

2. **Find the number of bits in the component memory.**

$$b_C = 128K \times 8 = 2^7 \times 2^{10} \times 2^3 = 2^{20} bits$$

3. **Find the number of RAM chips in the composite memory.**

$$N = \frac{2^{27}}{2^{20}} = 2^7 = 128$$

b) If we were addressing one full word, how many chips would be involved?

Solution:

Divide the number of bits at each address in the composite memory by the number of bits at each address in the component memory chips.

$$n = \frac{32}{8} = 4$$

c) How many address lines are needed for each RAM chip?

Solution:

Find the $\log_2 M$, where M is the number of address cells in the component RAM chips.

$$A = \log_2 128K = \log_2(2^7 \times 2^{10}) = \log_2 2^{17} = 17$$

d) How many banks will this memory have?

Solution:

The number of banks is equal to the number of component chips divided by the number of chips required to access a full word at a single address.

$$K = \frac{128}{4} = 32$$

e) How many address lines are needed for the composite memory?

Solution:

Find the $\log_2 M$, where M is the number of address cells in the composite memory.

$$A = \log_2 4M = \log_2(2^2 \times 2^{20}) = \log_2 2^{22} = 22$$