The CPU communicates with other components via a bus.

- A **bus** is a set of conductors (wires) that acts as a shared but common data path to connect multiple subsystems within the system.

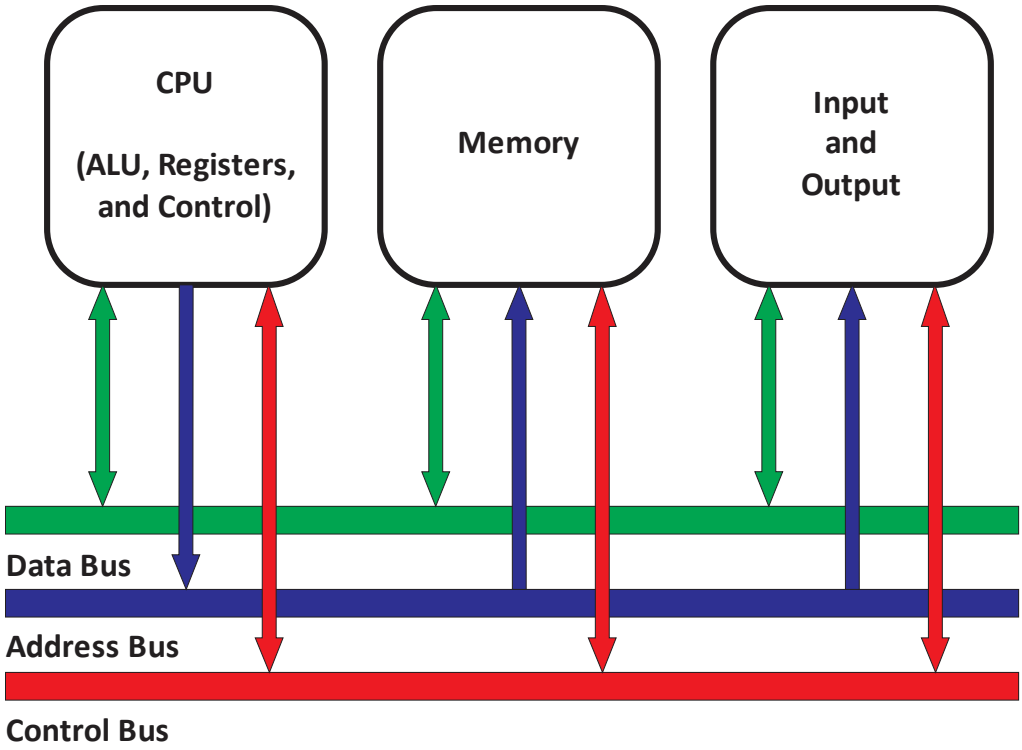

Figure 4.2 The Modified von Neumann Architecture, Adding a System Bus

- Buses consist of data lines, control lines, and address lines.
- While the data lines convey bits from one device to another, control lines determine the direction of data flow, and when each device can access the bus.
- Address lines determine the location of the source or destination of the data.

- Two types of buses are commonly found in computer systems: *point-to-point*, and *multipoint* buses.

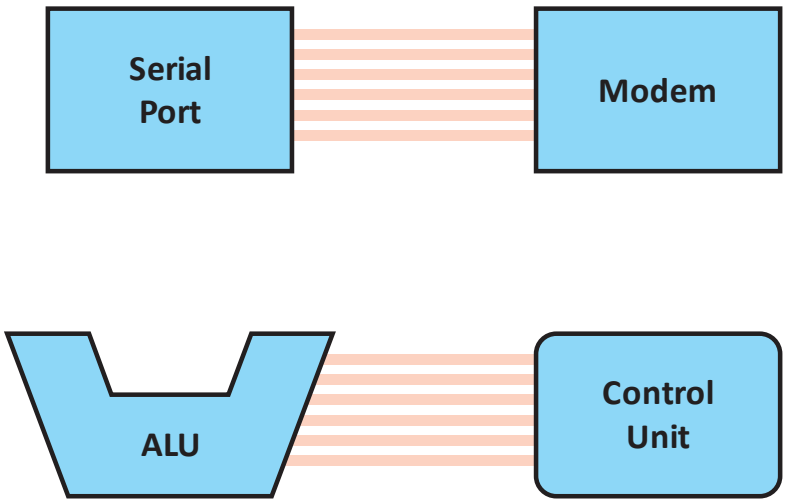

Figure 4.1 a) Point-to-Point Buses

Figure 4.1 b) Multipoint Bus

- Because a multipoint bus is a shared resource, access to it is controlled through protocols, which are built into the hardware.

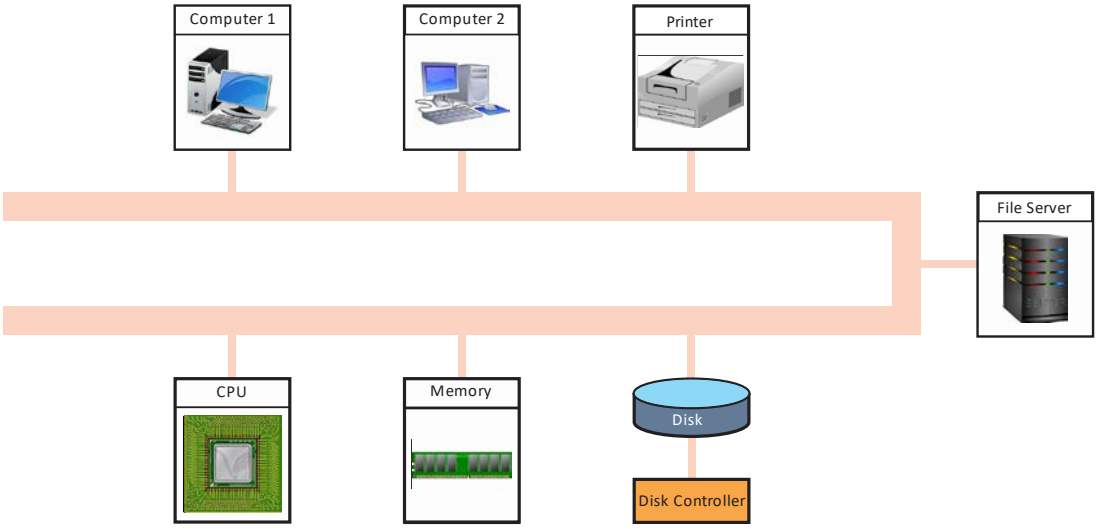

Figure 4.2 The Components of a Typical (Multipoint) Bus

- In a master-slave configuration, where more than one device can be the bus master, concurrent bus master requests must be arbitrated.
- Four categories of bus arbitration are:
  - **Daisy chain**: Permissions are passed from the highest-priority device to the lowest.
  - **Centralized parallel**: Each device is directly connected to an arbitration circuit.
  - **Distributed using self-detection**: Devices decide which gets the bus among themselves.
  - **Distributed using collision-detection**: Any device can try to use the bus. If its data collides with the data of another device, it tries again.
- **Processor-memory buses** are short, high-speed buses that are closely matched to the memory system on the machine to maximize the bandwidth (transfer of data) and are usually design specific.
- **I/O buses** are typically longer than processor-memory buses and allow for many types of devices with varying bandwidths. These buses are compatible with many different architectures. A backplane bus actually built into the chassis of the machine and connects to the processor, the I/O devices, and the memory (so all devices share on bus).

- **Synchronous buses** are clocked. Data and control transfers occur on the rising or falling edge of the clock. Every device is synchronized by the rate at which the clock ticks, or the **clock rate**.
- With **asynchronous buses**, control lines coordinate the operations, and a complex **handshaking protocol** must be used to enforce timing.

- An asynchronous protocol:
    1. ReqREAD: This bus control line is activated and the data memory address is put on the appropriate bus lines at the same time.
    2. ReadyDATA: This control line is asserted when the memory system has put the required data on the data lines for the bus.
    3. ACK: This control line is used to indicate that ReqREAD or the ReadyDATA has been acknowledged.
    - Using a protocol instead of the clock to coordinate transactions means that asynchronous buses scale better with technology and can support a wider variety of devices.