Computerized design tools exist to expedite and simplify logic design. Design tools need a Hardware Description Language (HDL). There are two such language commonly used, VHDL and Verilog. VHDL is an abbreviation for VHSIC Hardware Description Language and VHSIC means Very High Speed Integrated Circuit.

Of the two languages, Verilog is a little easier to understand. For example, the description of a half-adder is:

```
module hlfaddr (x,y,sum,car)
   input x;
   input y;
   output sum;
   output car;
   assign sum=x^y;
   assign car=x&y;
endmodule;
```

The Verilog ^ operator performs and exclusive OR and the Verilog & operator performs an AND.

Please note the similarity between the Verilog language and the C-based languages you have studied at UCO including C++ and Java.