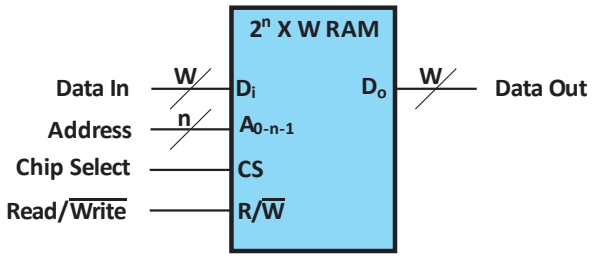
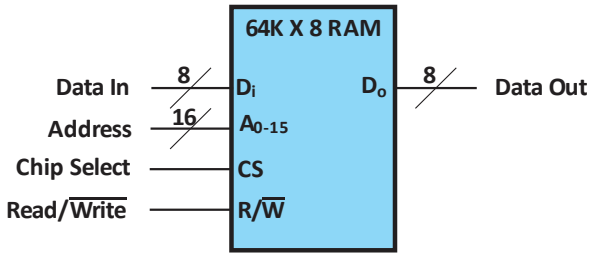


Generic Memory Block Diagram

Notes:

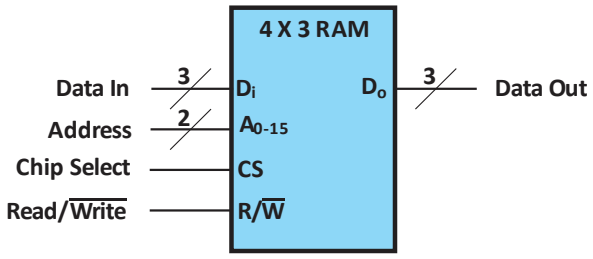
1. W: Number of *bits* stored at each address. The memory stores $W \times 2^n$ *bits*.
2. n: Number of address lines. The memory has 2^nlocations to store W bits.
3. D_i: Data in – data that will be stored at a particular address given by the Address lines.
4. D_o: Data out – data that are stored at a particular address given by the Address lines.
5. CS: Chip Select – when the chip is selected the memory is active. When the chip is not selected all input values, except the CS are ignored and the output values – Data Out – all have zero values.
6. $R/\overline{W}$: $Read/\overline{Write}$ – When $R/\overline{W} = 1$, all Data In values are blocked and the Data Out values at the given address are asserted on the Data Out lines. When $R/\overline{W} = 0$, the values on the Data In lines are stored at the given address in the memory.
7. RAM: Random Access Memory



64K X 8 Random Access Memory

Notes:

1. 64K means $2^{16} = 65{,}536 \neq 64{,}000$. This memory has 2^{16} memory locations.
2. Each memory location – each memory address stores eight (8) bits or one byte.



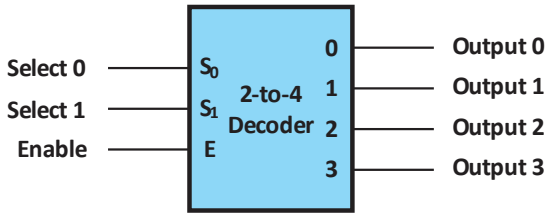
4 X 3 Random Access Memory

Notes:

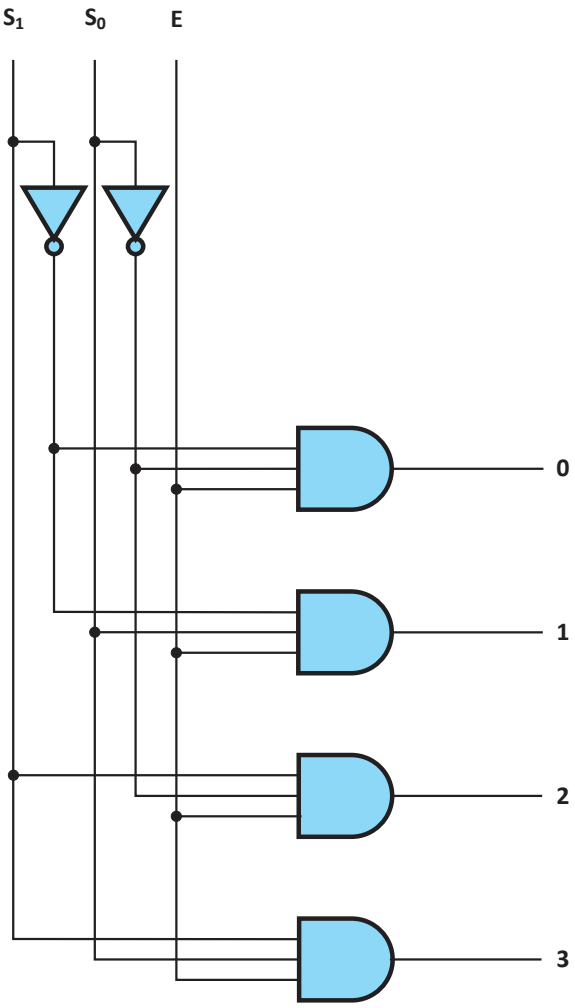
1. This memory has four (4) memory locations, each of which stores three (3) bits.

Design challenges.

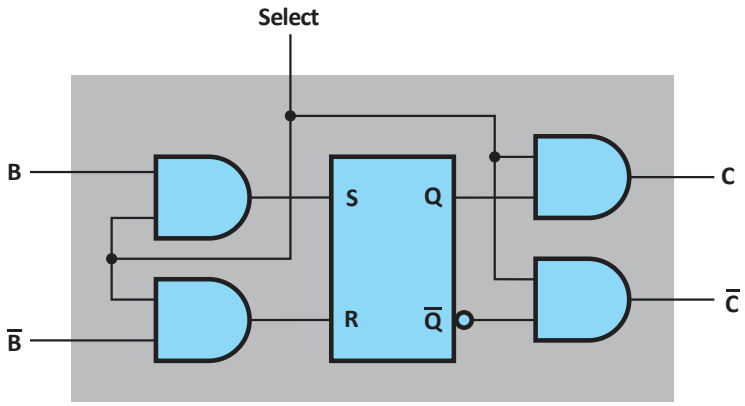
1. Decode the input address lines. Two input lines are decoded to four separate addresses.
2. Design logic that will select a single bit – that will select a single static RAM cell.
3. Design logic that will prevent input data from altering the memory when $R/\overline{W} = 1$ – when the memory is to be read.
4. Design a single bit memory cell with appropriate controls.



2-to-4 Decoder Block Diagram



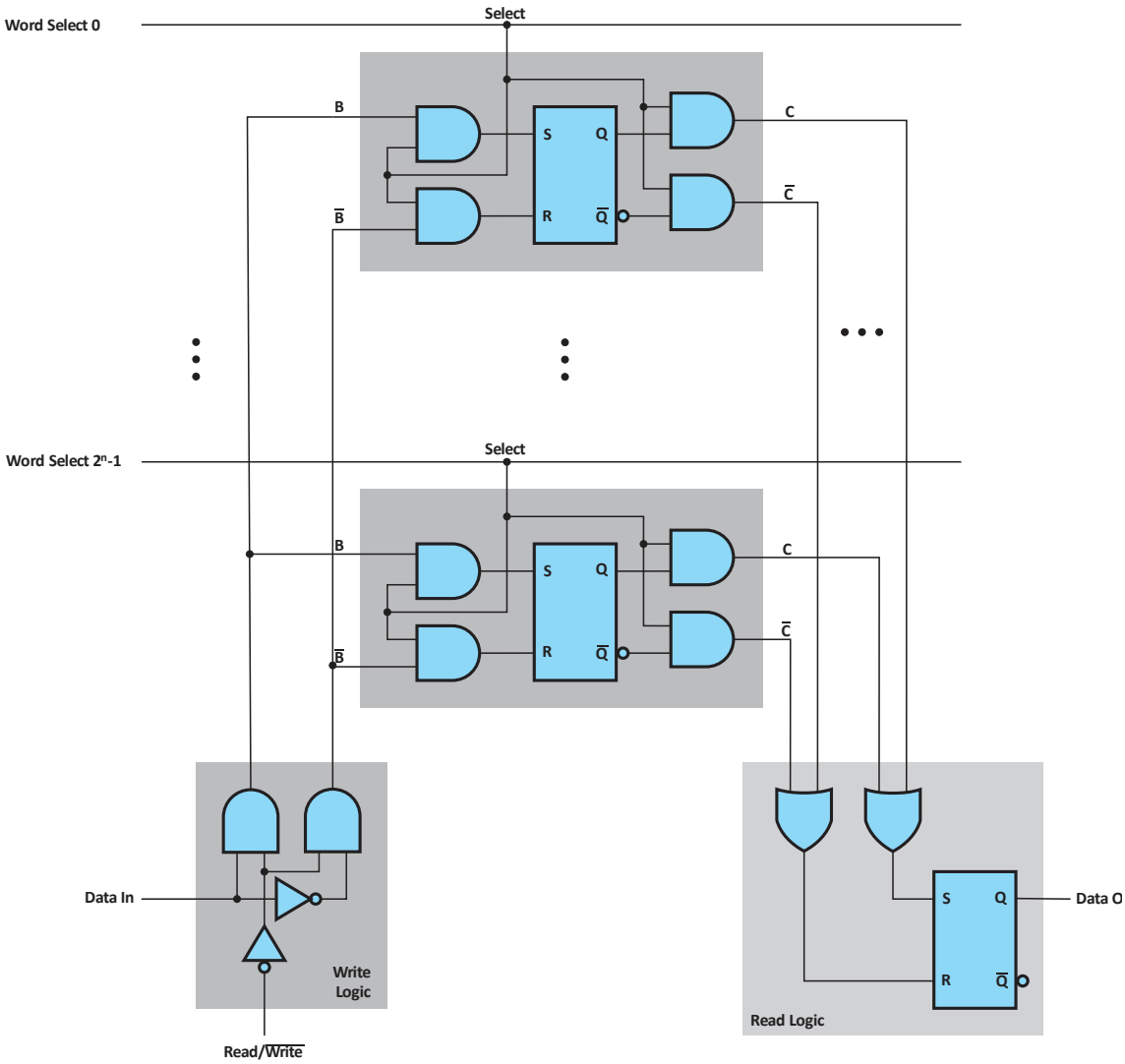
2-to-4 Decoder Logic Diagram



Static RAM Cell

Notes:

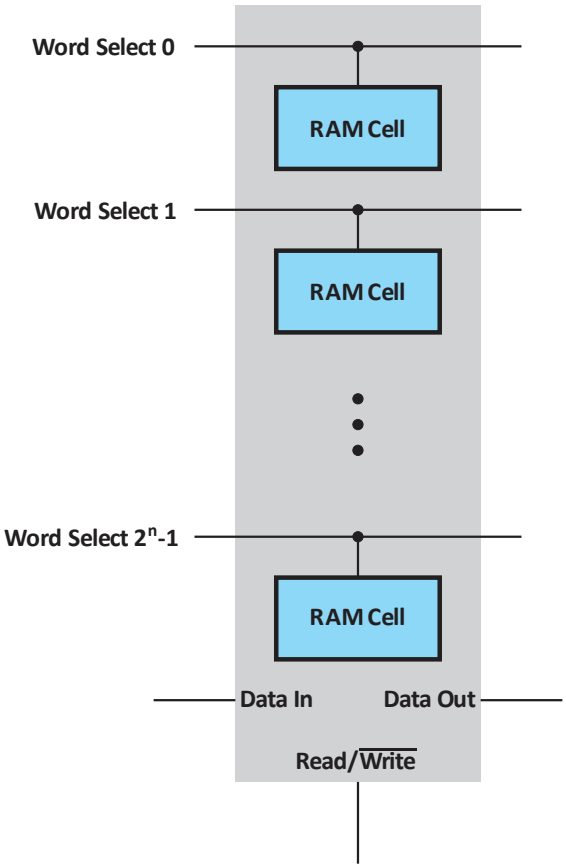
1. When $Select = 1$, input data values, B and $\overline{B}$, are stored in the SR Latch Flip-Flop and output values stored in the SR Latch, C and $\overline{C}$, are available.
2. Contrariwise, if $Select = 0$, both input and output data values are blocked.



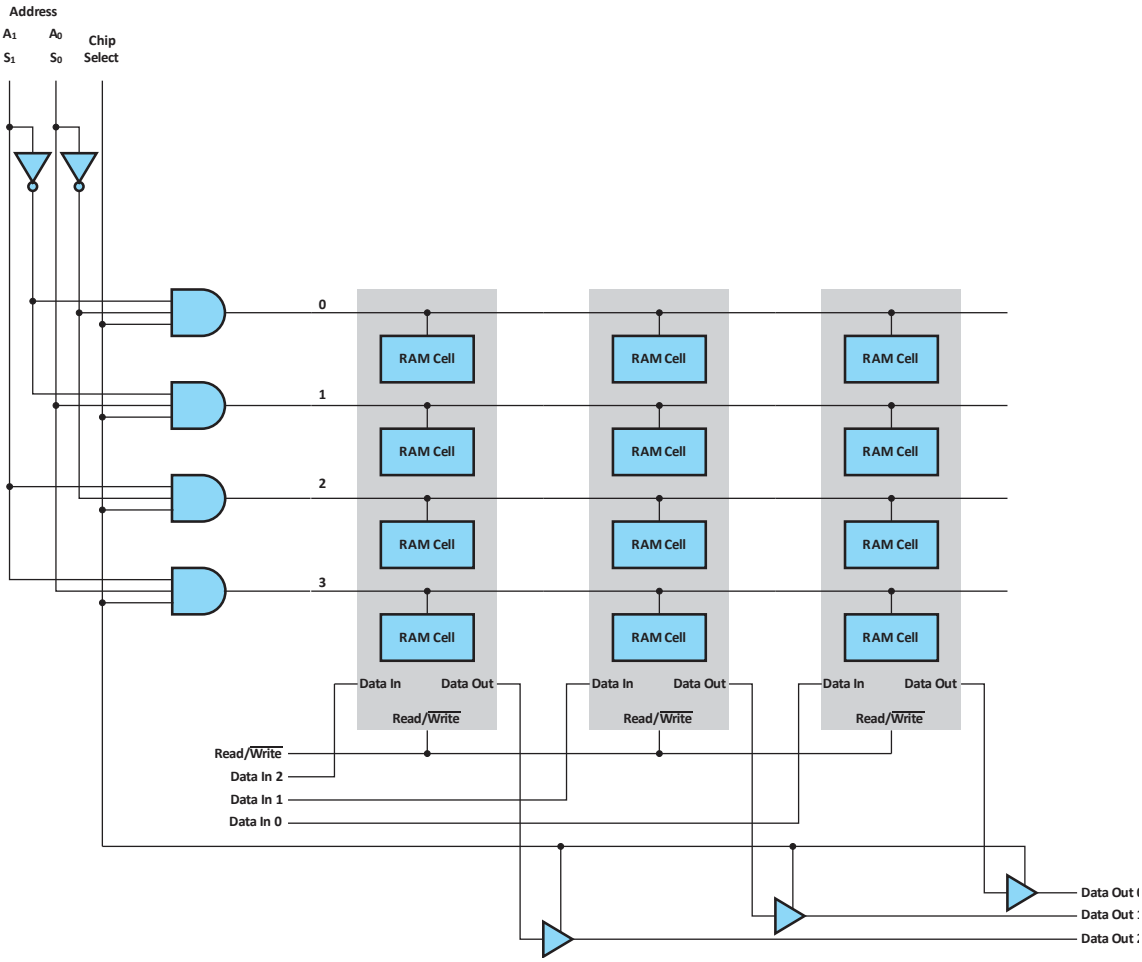
RAM Bit Slice Model Logic Diagram

Notes:

1. $Word\ Select\ x$ selects a row of static RAM cells. Each $Word\ Select$ line originates in the $n \times 2^n$ Decoder.
2. The Write Logic enables the capture of $Data\ In$ values when $Read/\overline{Write} = 1$ and blocks $Data\ In$ values when $Read/\overline{Write} = 0$.
3. The Read Logic captures the value read in the SR Latch.



RAM Bit Slice Model Symbol



4 X 3 Static RAM Block Diagram