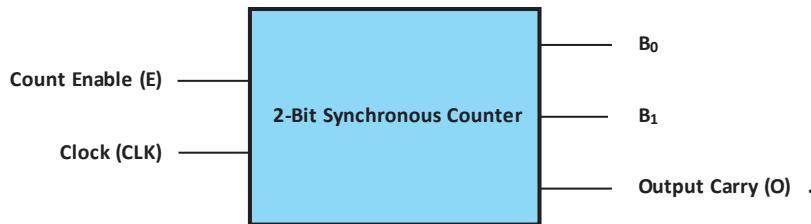
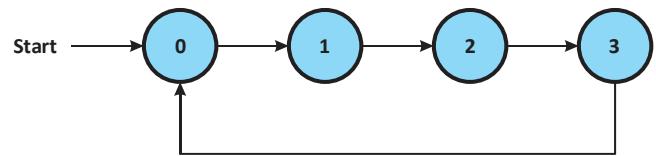


1. Read the problem specification and reduce to a block diagram.



2-Bit Synchronous Counter Block Diagram

2. Find the block that is a sequential circuit and draw a symbolic state diagram.



Simplified 2-Bit Synchronous Counter Symbolic State Diagram

3. Develop a symbolic PRESENT – NEXT STATE table.

PRESENT STATE	NEXT STATE
0	1
1	2
2	3
3	0

4. Determine the number of flip-flops, assign states, and revise the PRESENT – NEXT STATE table.

PRESENT STATE			NEXT STATE		
Symbolic	B_1	B_0	Symbolic	B_1	B_0
0	0	0	1	0	1
1	0	1	2	1	0
2	1	0	3	1	1
3	1	1	0	0	0

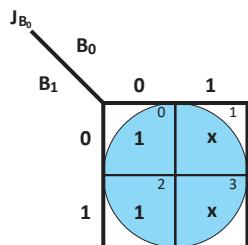
5. Develop a NEXT STATE DECODER for several kinds of flip-flops.

PRESENT STATE			NEXT STATE			NEXT STATE DECODER			
Symbolic	B_1	B_0	Symbolic	B_1	B_0	J_{B_1}	K_{B_1}	J_{B_0}	K_{B_0}
0	0	0	1	0	1	0	x	1	x
1	0	1	2	1	0	1	x	x	1
2	1	0	3	1	1	x	0	1	x
3	1	1	0	0	0	x	1	x	1

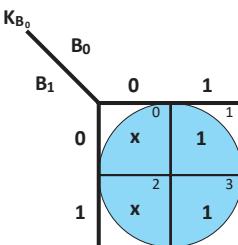
$Q(t)$	\rightarrow	$Q(t + 1)$	J	K
0		0	0	x
0		1	1	x
1		0	x	1
1		1	x	0

JK Excitation Table

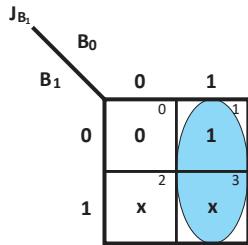
6. Plot the NEXT STATE DECODERS and determine which kind of flip-flop minimizes the logic for the NEXT STATE DECODER.



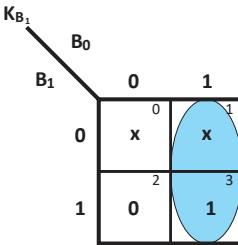
$$J_{B_0} = 1$$



$$K_{B_0} = 1$$

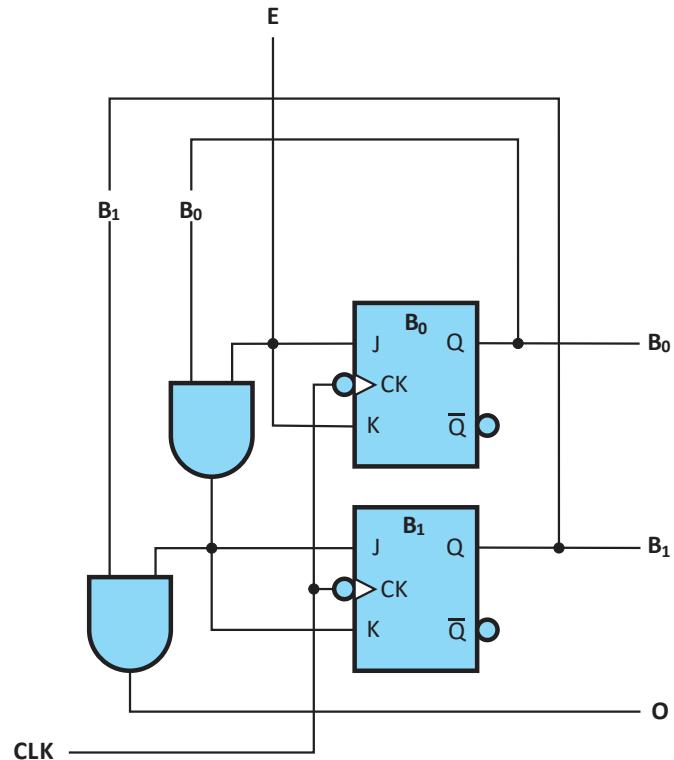


$$J_{B_1} = B_0$$

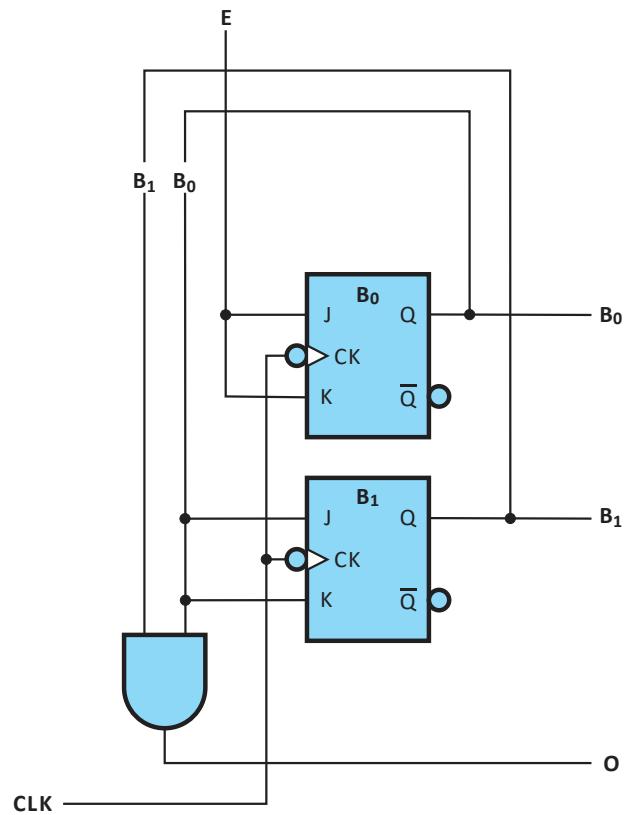


$$K_{B_1} = B_0$$

7. Draw the logic diagram.



Simplified Logic Diagram for a 2-Bit Synchronous Counter



Logic Diagram for a 2-Bit Synchronous Counter