Synchronous Sequential Circuit Design

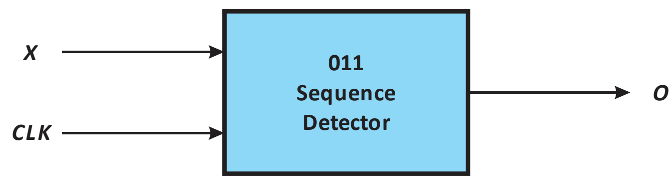
Steps:

1. Read the problem specification and reduce to a block diagram.
2. Find the block that is a sequential circuit and draw a symbolic state diagram.
3. Develop a symbolic PRESENT – NEXT STATE table.
4. Determine the number of flip-flops, assign states, and revise the PRESENT – NEXT STATE table.
5. Develop a NEXT STATE DECODER for several kinds of flip-flops.
6. Plot the NEXT STATE DECODERs and determine which kind of flip-flop minimizes the logic for the NEXT STATE DECODER.
7. Plot the output decoder logic.
8. Draw the logic diagram.

Example:

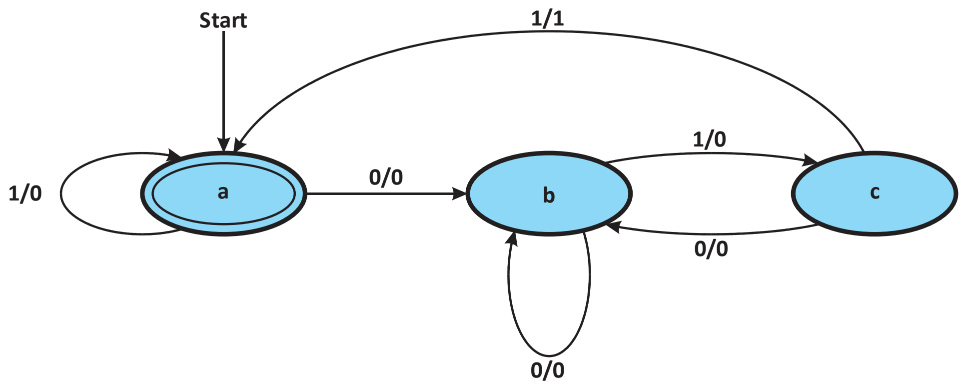
Problem Specification: Design a circuit that will produce an output one-pulse if it detects the binary sequence 011.

1. Read the problem specification and reduce to a block diagram.



Block Diagram
X: Input binary sequence
CLK: Clock
O: Output,
$O = 1$ if the binary sequence 011 has been detected
$O = 0$ if the binary sequence 011 has not been detected

2. Find the block that is a sequential circuit and draw a symbolic state diagram.



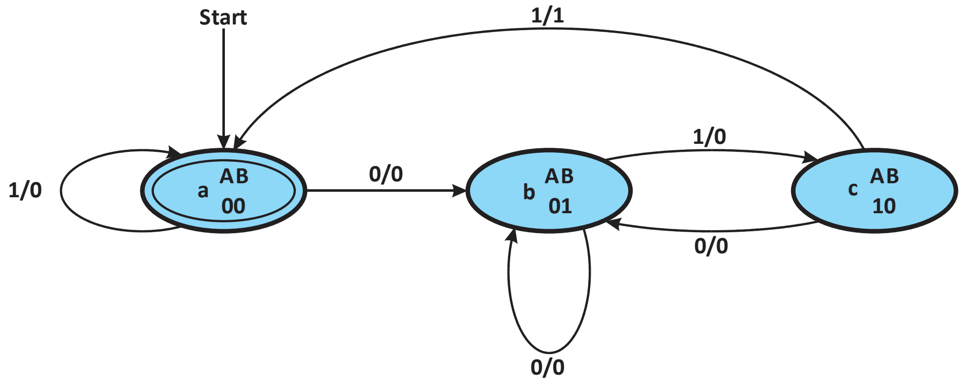
Symbolic State Diagram

3. Develop a symbolic PRESENT – NEXT STATE table.

Present State	Input X	Next State	Output O
a	0	b	0
	1	a	0
b	0	b	0
	1	c	0
c	0	b	0
	1	a	1

Symbolic Present-State-Next-State Table

4. **Determine the number of flip-flops, assign states, and revise the PRESENT – NEXT STATE table.**



State Diagram

Present State			Input	Next State			Output
Symbolic	A	B	X	Symbolic	A	B	O
a	0	0	0	b	0	1	0
	0	0	1	a	0	0	0
b	0	1	0	b	0	1	0
	0	1	1	c	1	0	0
c	1	0	0	b	0	1	0
	1	0	1	a	0	0	1
	1	1	0	X	X	X	X
	1	1	1	X	X	X	X

Present-State-Next-State Table

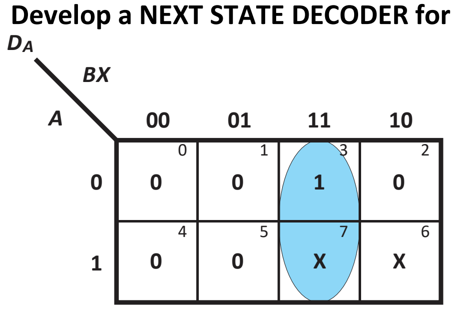
5. **Plot the NEXT STATE DECODERs and determine which kind of flip-flop minimizes the logic for the NEXT STATE DECODER.**

Present State			Input	Next State			Output	Next State Decoder					
Sym	A	B	X	Sym	A	B	O	J_A	K_A	J_B	K_B	D_A	D_B
a	0	0	0	b	0	1	0	0	X	1	X	0	1
	0	0	1	a	0	0	0	0	X	0	X	0	0
b	0	1	0	b	0	1	0	0	X	X	0	0	1
	0	1	1	c	1	0	0	1	X	X	1	1	0
c	1	0	0	b	0	1	0	X	1	1	X	0	1
	1	0	1	a	0	0	1	X	1	0	X	0	0
	1	1	0	X	X	X	X	X	X	X	X	X	X
	1	1	1	X	X	X	X	X	X	X	X	X	X

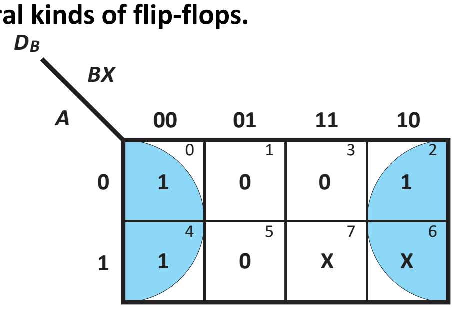
$Q(t)$	$\rightarrow$	$Q(t+1)$	J	K
0		0	0	X
0		1	1	X
1		0	X	1
1		1	X	0

JK Flip-Flop Excitation Table

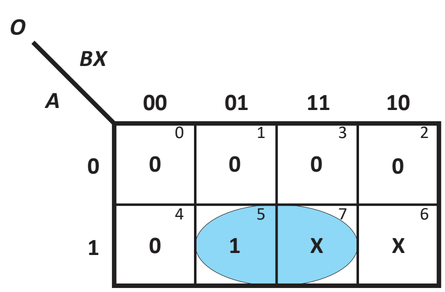
6. **Develop a NEXT STATE DECODER for several kinds of flip-flops.**



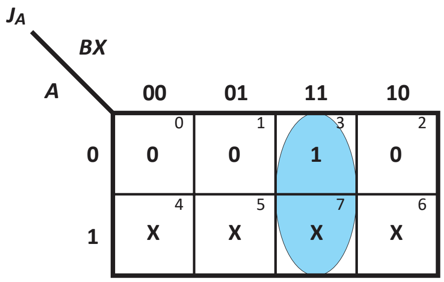
$D_A = BX$



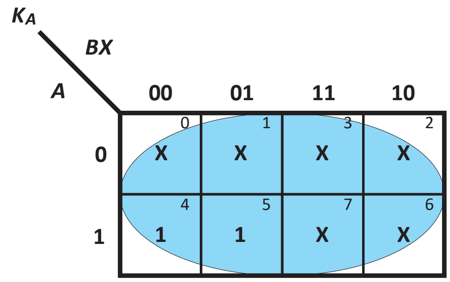
$D_B = \overline{X}$



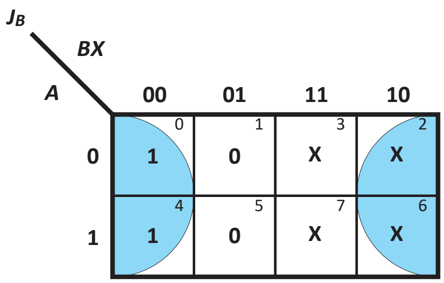
$O = AX$



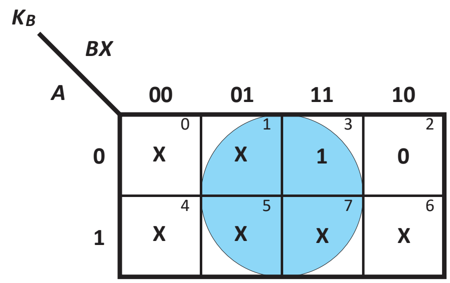
$J_A = BX$



$K_A = 1$

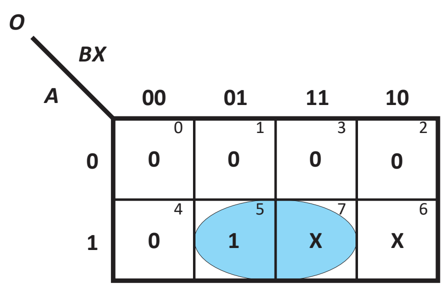


$J_B = \overline{X}$



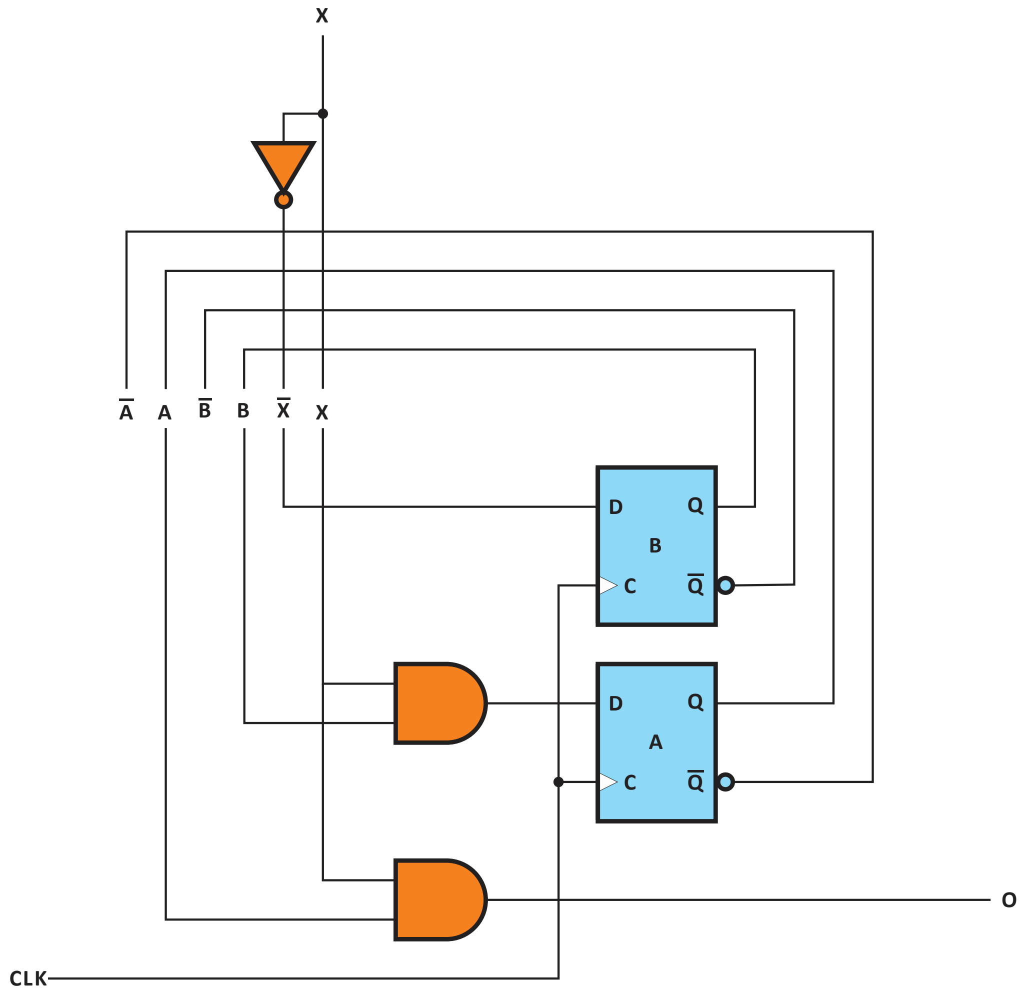
$K_B = X$

7. **Plot the output decoder logic.**



$O = AX$

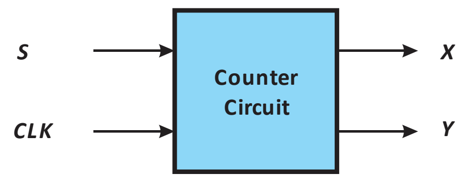
8. **Draw the logic diagram.**



Logic Diagram

Problem Specification: Design a counter that when switch S is off (0), counts 0, 2, 0, 2, …, and when the switch is on (1), counts 1, 3, 1, 3, … . When the counter is in state 0 and the switch is on (1), the counter switches to an odd state. When the counter is in state 1 and the switch is off (0), counter switches to an even state. Define two outputs X and Y such that they display the values of the counter in binary. For example, when the counter is in state 1, $XY = 01$, that is, $X = 0$ and $Y = 1$.

1. Read the problem specification and reduce to a block diagram.

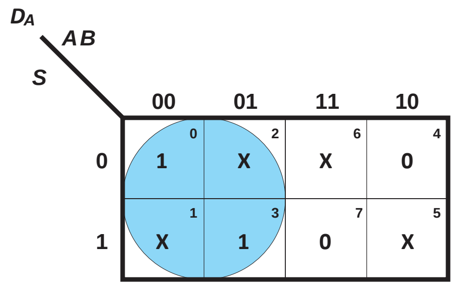


Block Diagram

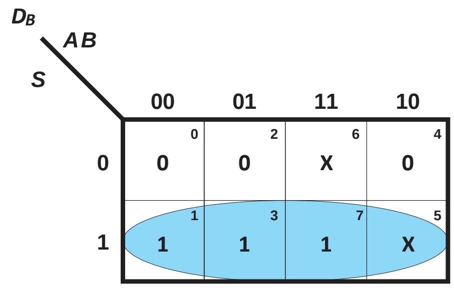
1.1. Analyze the problem

$\#$	A	B	S	$\#$	A	B	

Present State			Input	Next State			
#	***A***	***B***	***S***	**#**	***A***	***B***	
0	0	0	0	2	1	0	$S = 0, 0 \rightarrow 2$
0	0	0	1		X	1	$S = 1, 0 \rightarrow odd$
1	0	1	0		X	0	$S = 0, 1 \rightarrow even$
1	0	1	1	3	1	1	$S = 1, 1 \rightarrow 3$
2	1	0	0	0	0	0	$S = 0, 2 \rightarrow 0$
2	1	0	1		X	1	
3	1	1	0		X	0	
3	1	1	1	1	0	1	$S = 1, 3 \rightarrow 1$



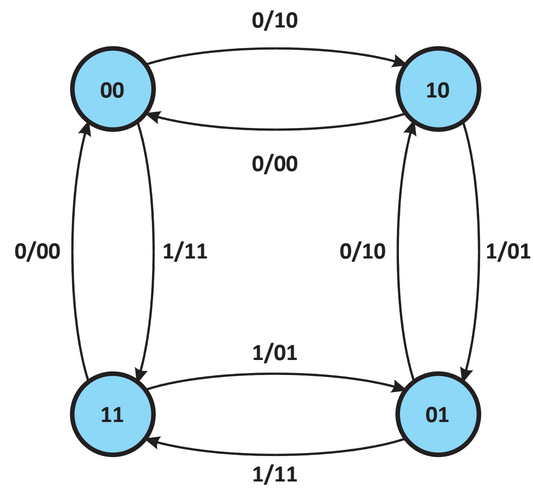
$D_A = \overline{A}$



$D_B = S$

Present State			Input	Next State			Output	
#	*A*	*B*	*S*	#	*A*	*B*	*X*	*Y*
0	0	0	0	2	1	0		
0	0	0	1	3	1	1		
1	0	1	0	2	1	0		
1	0	1	1	3	1	1		
2	1	0	0	0	0	0		
2	1	0	1	1	0	1		
3	1	1	0	0	0	0		
3	1	1	1	1	0	1		

2. Find the block that is a sequential circuit and draw a symbolic state diagram.



Symbolic State Diagram
Well, it is not too symbolic

3. Develop a symbolic PRESENT – NEXT STATE table.

Present State			Input	Next State			Output	
#	*A*	*B*	*S*	#	*A*	*B*	*X*	*Y*
0	0	0	0	2	1	0	1	0
0	0	0	1	3	1	1	1	1
1	0	1	0	2	1	0	1	0
1	0	1	1	3	1	1	1	1
2	1	0	0	0	0	0	0	0
2	1	0	1	1	0	1	0	1
3	1	1	0	0	0	0	0	0
3	1	1	1	1	0	1	0	1

4. Determine the number of flip-flops, assign states, and revise the PRESENT – NEXT STATE table.

- Yes, we already did that task.

5. **Plot the NEXT STATE DECODERs and determine which kind of flip-flop minimizes the logic for the NEXT STATE DECODER.**

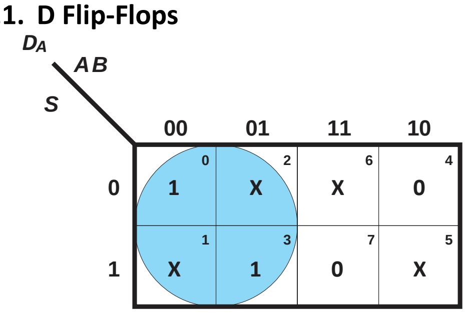
Present State		Input	Next State		Next State Decoder					
A	B	S	A	B	D_A	D_B	J_A	K_A	J_B	K_B
0	0	0	1	0	1	0	1	X	0	X
0	0	1	1	1	1	1	1	X	1	X
0	1	0	1	0	1	0	1	X	X	1
0	1	1	1	1	1	1	1	X	X	0
1	0	0	0	0	0	0	X	1	0	X
1	0	1	0	1	0	1	X	1	1	X
1	1	0	0	0	0	0	X	1	X	1
1	1	1	0	1	0	1	X	1	X	0

$Q(t)$	$\rightarrow$	$Q(t+1)$	J	K
0		0	0	X
0		1	1	X
1		0	X	1
1		1	X	0

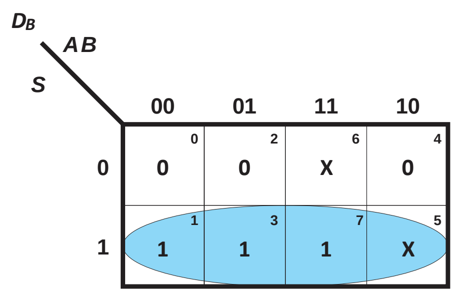
JK Flip-Flop Excitation Table

6. **Develop a NEXT STATE DECODER for several kinds of flip-flops.**

6.1. D Flip-Flops



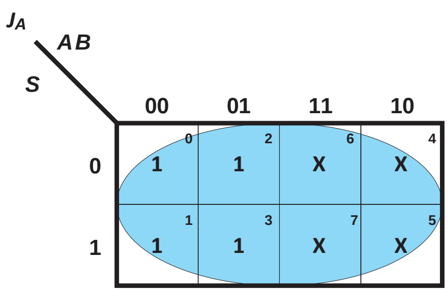
$D_A = \overline{A}$



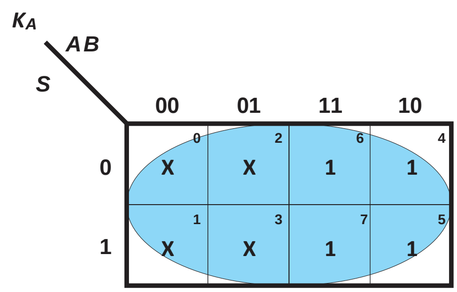
$D_B = S$

6.2. JK Flip-Flops

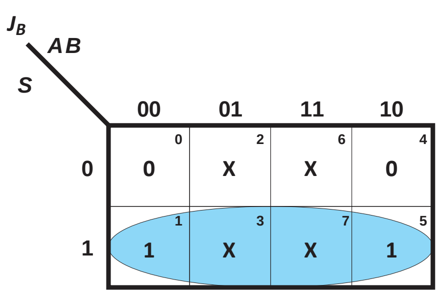
Present State		Input	Next State		Next State Decoder					
A	B	S	A	B	D_A	D_B	J_A	K_A	J_B	K_B
0	0	0	1	0	1	0	1	X	0	X
0	0	1	1	1	1	1	1	X	1	X
0	1	0	1	0	1	0	1	X	X	1
0	1	1	1	1	1	1	1	X	X	0
1	0	0	0	0	0	0	X	1	0	X
1	0	1	0	1	0	1	X	1	1	X
1	1	0	0	0	0	0	X	1	X	1
1	1	1	0	1	0	1	X	1	X	0



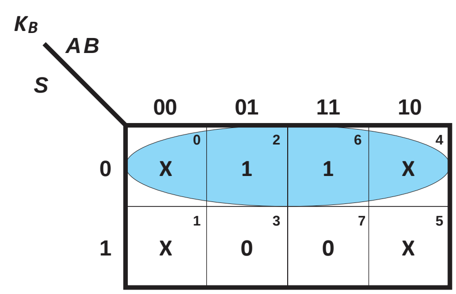
$J_A = 1$



$K_A = 1$



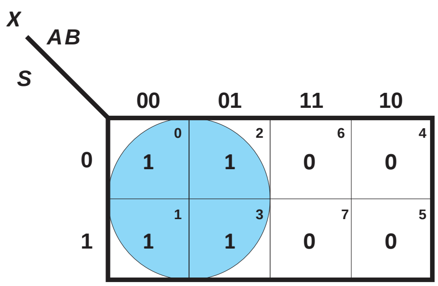
$J_B = S$



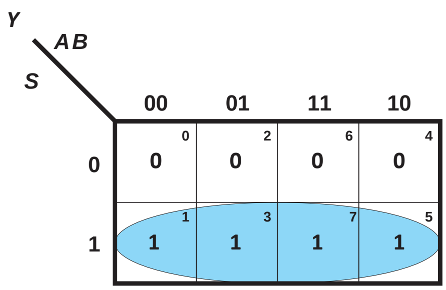
$K_B = \overline{S}$

7. **Plot the output decoder logic.**

	Present State		Input	Next State			Output	
#	A	B	S	A	B	#	X	Y
0	0	0	0	1	0	2	1	0
0	0	0	1	1	1	3	1	1
1	0	1	0	1	0	2	1	0
1	0	1	1	1	1	3	1	1
2	1	0	0	0	0	0	0	0
2	1	0	1	0	1	1	0	1
3	1	1	0	0	0	0	0	0
3	1	1	1	0	1	1	0	1

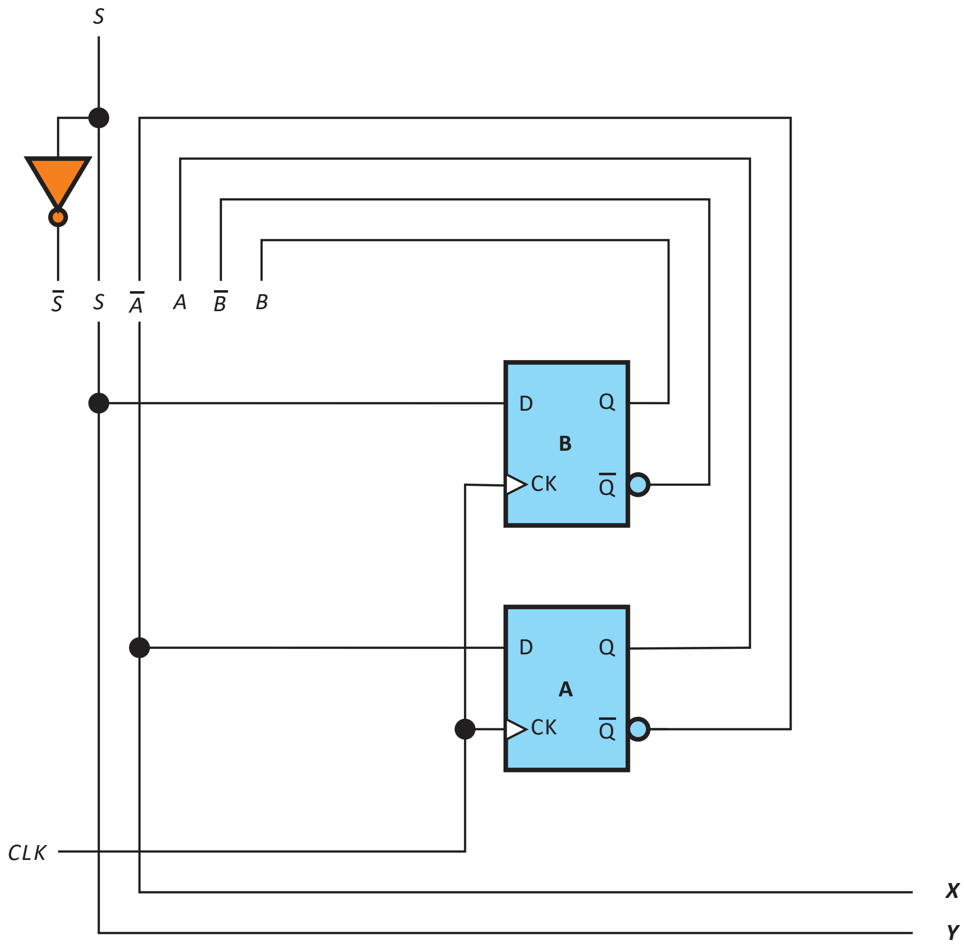


$X = \overline{A}$



$Y = S$

8. **Draw the logic diagram.**



Logic Diagram