1. Feedback
2. Cross-coupled NOR Gates
3. Cross-coupled NAND Gates
4. Clocks and Flip-Flops
5. Ad-hoc design of a SR Flip-Flop
6. Characteristic Table
7. Truth Table
8. Excitation Table

- Memory is implemented by employing feedback.

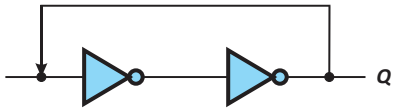


FIGURE 3.29 Example of Simple Feedback

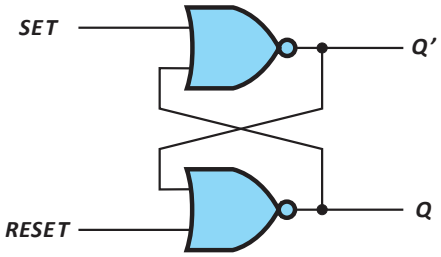


FIGURE 3.31 (a) Binary Cell implemented using cross coupled NOR gates

Inputs		**Present State**	**Next State**
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	undefined
1	1	1	undefined

Table 3.31 (a) Cross-coupled NOR gate Binary Cell Characteristic Table

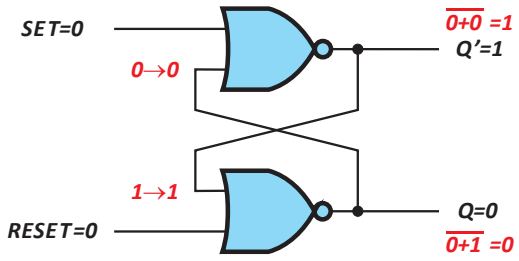


FIGURE 3.31 (a-1) Binary Cell implemented using cross coupled NOR gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	0	0	0

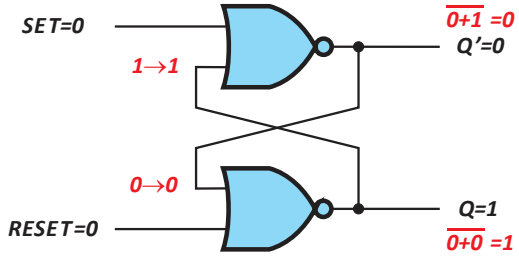


FIGURE 3.31 (a-2) Binary Cell implemented using cross coupled NOR gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	0	1	1

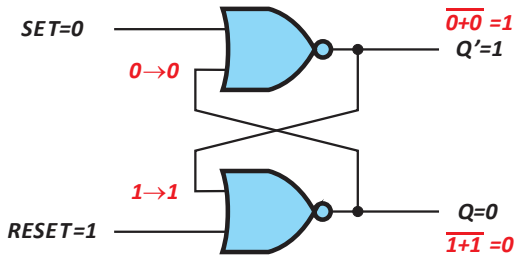


FIGURE 3.31 (a-3) Binary Cell implemented using cross coupled NOR gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	1	0	0

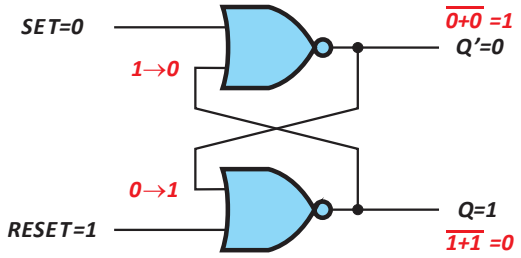


FIGURE 3.31 (a-4) Binary Cell implemented using cross coupled NOR gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	1	1	0

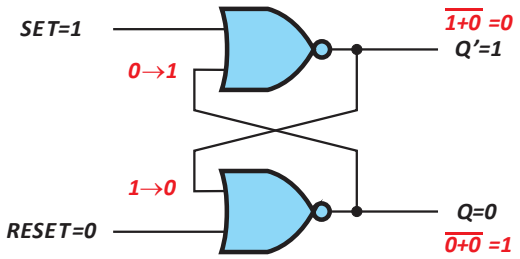


FIGURE 3.31 (a-5) Binary Cell implemented using cross coupled NOR gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
1	0	0	1

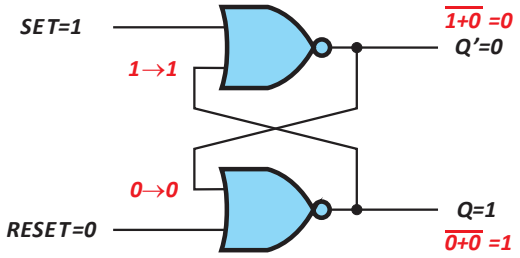
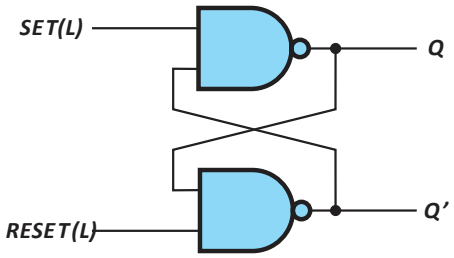


FIGURE 3.31 (a-6) Binary Cell implemented using cross coupled NOR gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
1	0	1	1

- Binary Cell Characteristics (implemented using cross-coupled NAND gates)
  - When $SET = RESET = 1$, the Binary Cell retains its original state.
  - When $SET = \mathbf{0}$ and $RESET = 1$, $Q = 1$ – the Binary Cell is set.
  - When $SET = 1$ and $RESET = \mathbf{0}$, $Q = 0$ – the Binary Cell is reset.
  - When $SET = 0$ and $RESET = 0$, $Q = ?$ – Invalid control: Don't do.



Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	0	0	undefined
0	0	1	undefined
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Table 3.32 (a) Cross-coupled NAND gate Binary Cell Characteristic Table

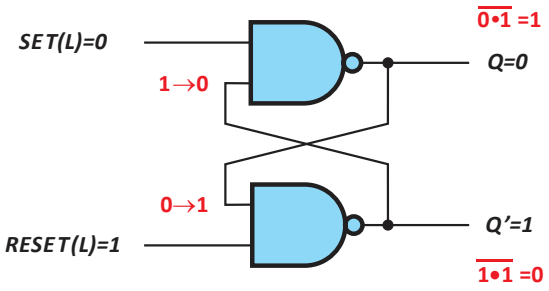


Figure 3.32 (a-1) Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	1	0	1

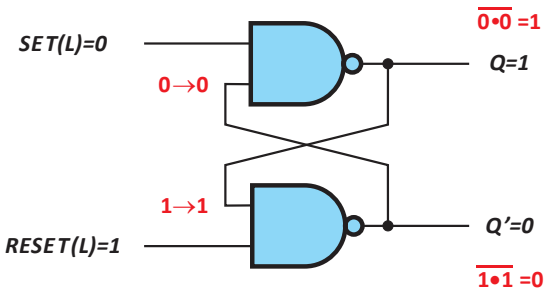


Figure 3.32 (a-2) Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
0	1	1	1

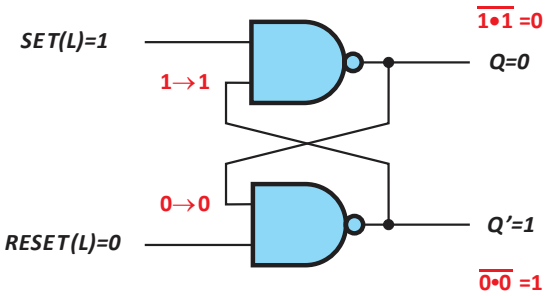


Figure 3.32 (a-3) Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
1	0	0	0

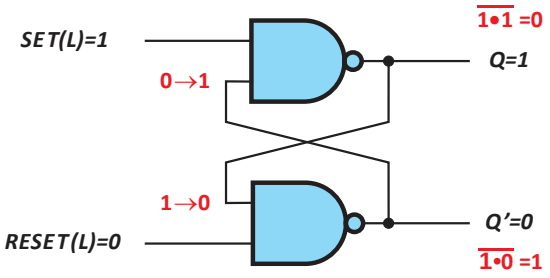


Figure 3.32 (a-4) Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
1	0	1	0

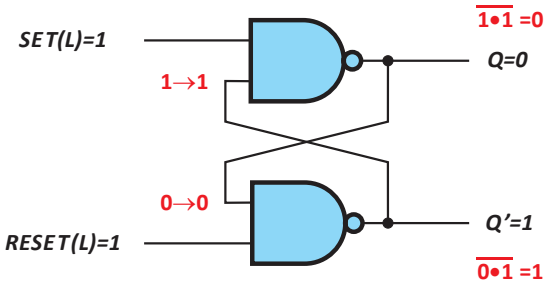


Figure 3.32 (a-5) Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
1	1	0	0

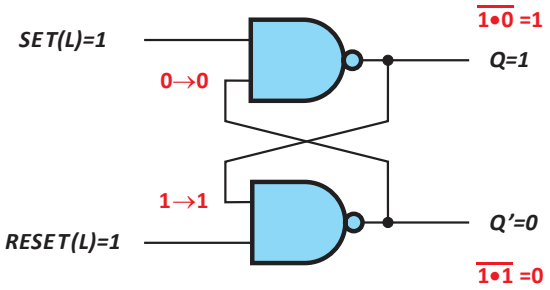


Figure 3.32 (a-6) Binary Cell implemented using cross coupled NAND gates

Inputs		Present State	Next State
SET	$RESET$	$Q(t)$	$Q(t+1)$
1	1	1	1