A multiplexer is a circuit that permits the designer to select a signal on one conductor from among many conductors.

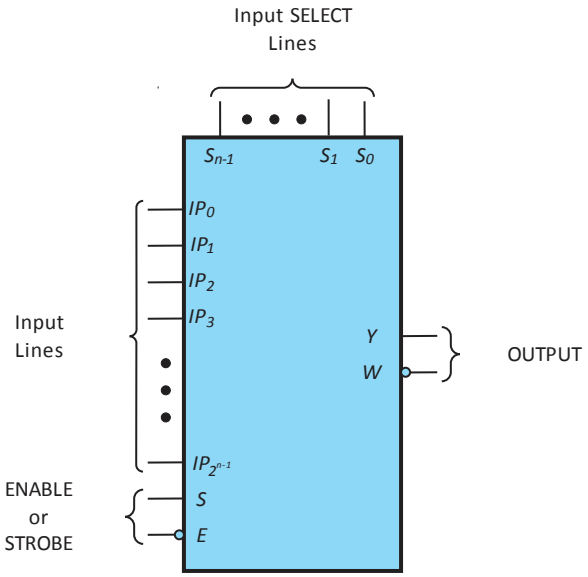

Figure 3.24 (b) A Multiplexer Symbol
The general schematic model for the 2^n-to-1 MUX

Notes

- There are 2^n input IP_i lines where $n = 1,2,3,4$, typically.
- There are n select $S_i$lines where n has the same value as given in the input lines above.
- The unsigned binary integer value of the select lines, taken as a group, where S_{n-1} is the most significant bit and S_0 is the least significant bit, identifies the input line that connected to the Y-output line.

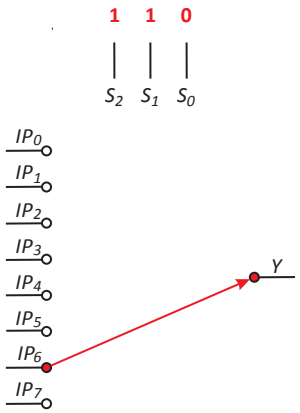

Figure 2. Multiplexer Functional Characteristics.
Selectors $S_2S_1S_0 = 110_2 = 6$ connect IP_6 to the Y-output.

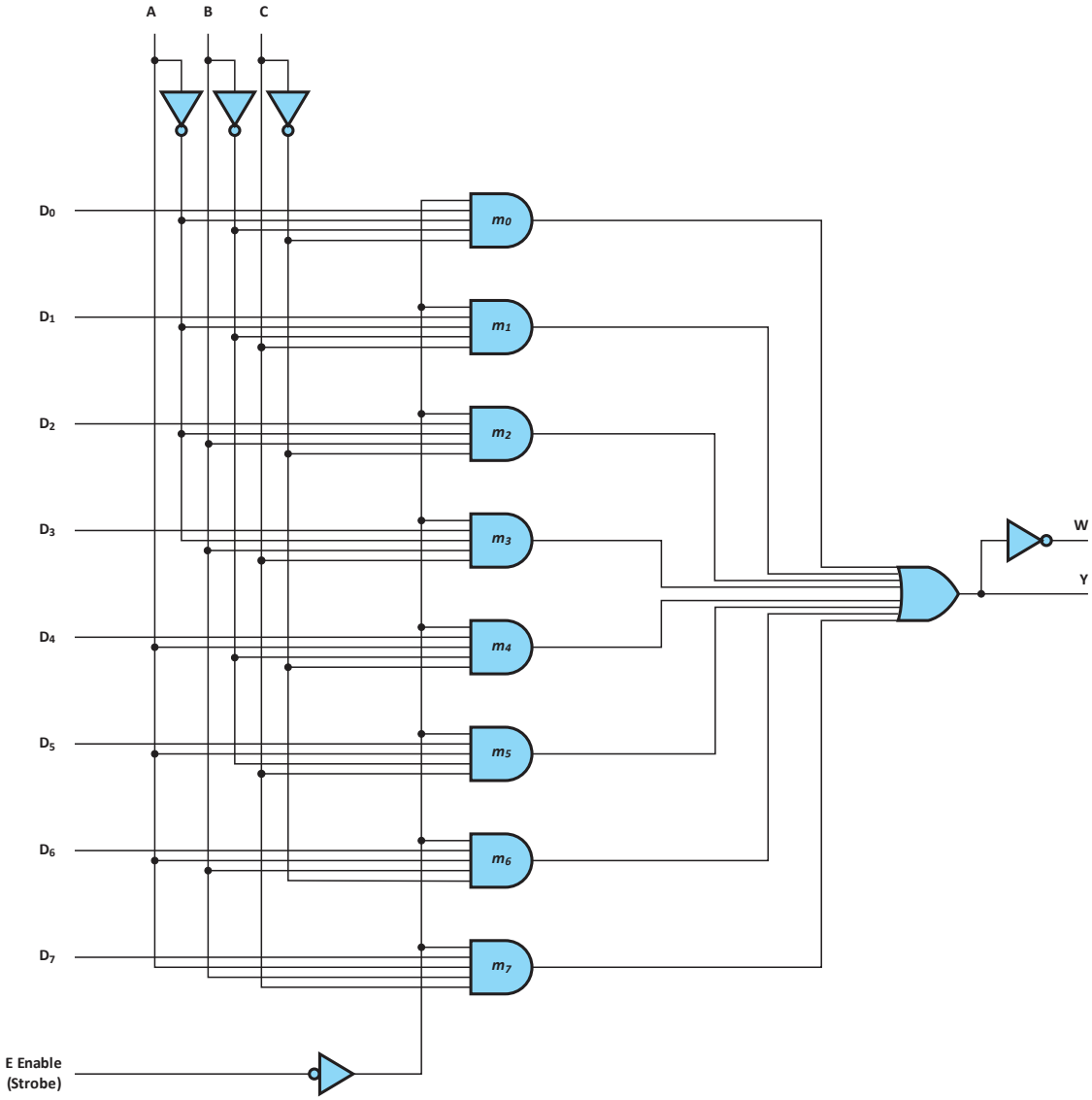

Figure 3.24 (a) A Look Inside a Multiplexer
3 × 8 MUX

$$Y = m_0(D_0) + m_1(D_1) + \cdots + m_7(D_7)$$

m_i	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	0
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	0

Figure 3. Function $F(A, B, C, D)$

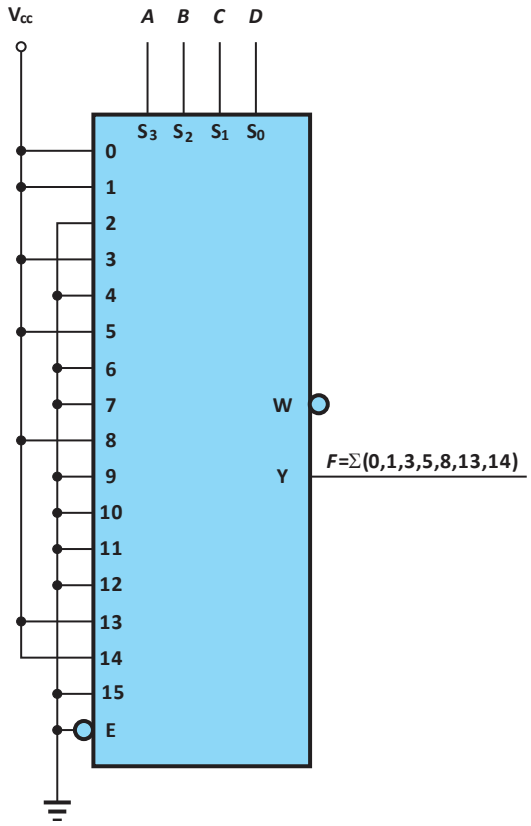

Figure 4. MUX implementation of Function $F(A, B, C, D)$ given in Figure 3.

m_i	A	B	C	D	F	F
0	0	0	0	0	1	1
1	0	0	0	1	1	
2	0	0	1	0	0	D
3	0	0	1	1	1	
4	0	1	0	0	0	D
5	0	1	0	1	1	
6	0	1	1	0	0	0
7	0	1	1	1	0	
8	1	0	0	0	1	D'
9	1	0	0	1	0	
10	1	0	1	0	0	0
11	1	0	1	1	0	
12	1	1	0	0	0	D
13	1	1	0	1	1	
14	1	1	1	0	1	D'
15	1	1	1	1	0	

Figure 4. Function

$$F(A,B,C,D) = m_0 \cdot 1 + m_1 \cdot D + m_2 \cdot D + m_3 \cdot 0 + m_4 \cdot D' + m_5 \cdot 0 + m_6 \cdot D + m_7 \cdot D'$$