1. Print your name on your scantron in the space labeled NAME.
2. Print CMSC 3833 in the space labeled SUBJECT.
3. Print the date 12-9-2013, in the space labeled DATE.
4. Print your CRN, 21858, in the space labeled PERIOD.
5. Print the test number and version, T3/V1, in the space labeled TEST NO.
6. Mark the best selection that satisfies the question. If selection b is better that selections a and d, then mark selection b. Mark only one selection.
7. Darken your selections completely. Make a heavy black mark that completely fills your selection.
8. Answer all 40 questions.
9. Record your answers on SCANTRON form 882-E (It is green!)
10. Submit your completed scantron on Monday, December 9, 2013 at 7:30 p.m. in MCS 111.
1. A 512K X 8 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. Assume that the RAM cell array is square. How many AND gates are required to decode an address?

a. 2304  
b. 2112  
c. 2176  
d. 2560

2. Which sequence is implemented by the logic diagram in the figure below given that the triple ABC, a binary value, is converted to decimal?

![Logic Diagram]

a. 0,2,4,6,0  
b. 0,4,2,6,0  
c. 0,6,4,2,0  
d. 0,2,6,4,0
3. Given that $R1=11001011$ and $R2=00001111$ find the result of the following sequentially executed micro-operations:
   1. $R1 \leftarrow sr R1$
   2. $R1 \leftarrow sl R1$
   3. $R1 \leftarrow R1 \cap R2$.
      a. 00001111
      b. 00001011
      c. 00001110
      d. 00001101

4. A 16K X 16 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. Assume that the RAM cell array is square. How many rows are there in the RAM cell array?
   a. 10
   b. 9
   c. $2^{10}$
   d. $2^9$

5. A 64K X 16 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. Assume that the RAM cell array is square. Determine the address on the column selection lines when the entire input address is $(15,099)_{10}$.
   a. 111101
   b. 0011101011
   c. 0011100111
   d. 111011
6. Select the correct equation for $D_i$ for the single stage of a register shown in figure 7.

\[ D_i = S_1 \cdot S_0 \cdot Q_{i-1} + S_1 \cdot S_0 \cdot Q_i + S_1 \cdot S_0 \cdot Q_{i+1} + S_1 \cdot S_0 \cdot I \]

7. How many address lines and input-output data lines are needed for a memory specified as 4M X 2?

a. 19 address lines; 16 I/O data lines.
b. 20 address lines; 8 I/O data line.
c. 21 address lines; 4 I/O data line.
d. 22 address lines; 2 I/O data lines.
8. A 256K X 16 RAM chip uses coincident decoding by splitting the internal decoder into row-select and column select. Assume that the RAM cell array is square. How many bits are in the array?

a. 4 million
b. 2 million
c. $2^{22}$
d. 256K

9. Which operation was performed on the two 8-bit operands 11001001 and 10100101 to obtain the result 10000001?

a. XOR
b. AND
c. OR
d. NOR

10. How many address lines and input-output data lines are needed for a memory specified as 64M X 64?

a. 32 address lines; 32 I/O data lines.
b. 16 address lines; 26 I/O data lines.
c. 64 address lines; 64 I/O data lines.
d. 26 address lines; 64 I/O data lines.

11. A composite memory is constructed from 16K X 4 memory chips and a decoder. How many chips are needed for a 128K X 8 memory?

a. 16
b. 8
c. 4
d. 32

12. A 128K X 8 RAM chip uses coincident decoding by splitting the internal decoder into row select and column select. Assume that the RAM cell array is square. What is the size of the column-decoder?

a. 6
b. $2^7$
c. $2^6$
d. 16
13. Design the logic for a single stage of a register that has the following register transfer functions.

\[ C_0: B \leftarrow A \cup B \]
\[ C_1: B \leftarrow A \cap \overline{B} \]

Find the optimum logic using AND, OR, and NOT gates for the D input to the D flip-flop in the cell.

a. \[ D_i = \overline{C_0} \cdot B_i + C_1 \cdot \overline{C_0} \cdot A_i + C_0 \cdot A_i \cdot \overline{B_i} \]
b. \[ D_i = \overline{C_1} \cdot \overline{C_0} \cdot B_i + C_1 \cdot \overline{C_1} \cdot C_0 \cdot (A_i + B_i) + C_1 \cdot \overline{C_0} \cdot (A_i \cdot \overline{B_i}) \]
c. \[ D_i = \overline{C_0} \cdot \overline{C_1} \cdot B_i + C_0 \cdot \overline{C_1} \cdot \overline{B_i} + C_0 \cdot \overline{C_1} \cdot A_i + C_0 \cdot A_i \cdot \overline{B_i} \]
d. \[ D_i = \overline{C_1} \cdot B_i + C_0 \cdot \overline{C_1} \cdot A_i + C_1 \cdot A_i \cdot \overline{B_i} \]

14. Select the equations that write data bit \( D \) to the Static RAM Cell shown below.

\[ \text{Static RAM Cell} \]

\[ B \]
\[ \overline{B} \]
\[ K \]
\[ C \]
\[ \overline{C} \]

a. \( B = KD, \overline{B} = K \overline{D} \)
b. \( B = \overline{KD}, \overline{B} = \overline{K} \cdot \overline{D} \)
c. \( S = KD, R = K \overline{D} \)
d. \( S = \overline{KD}, R = \overline{K} \cdot \overline{D} \)
15. Select the correct Write-Logic model for the diagram of the Partial RAM Bit Slice Model.
16. Why must address lines be stable before Read/Write is asserted low (0).

![Write cycle diagram]

- Address lines must be stable so that the CPU clock is not made asynchronous.
- Address lines must be stable so that the operation is completed in the required four clock cycles.
- Address lines must be stable so that data are written to the address specified and no other address.
- Address lines must be stable so handshaking sequence is properly implemented.

17. Identify the components of a dynamic RAM cell.

- A dynamic RAM cell consists of a transistor and a capacitor.
- A dynamic RAM cell consists of two transistors.
- A dynamic RAM cell consists of a transistor and a resistor.
- A dynamic RAM cell consists of a transistor and an inductor.

18. A DRAM has a refresh interval of 64 ms and has 8192 rows. What is the interval between refreshes for distributed refresh?

- 7.81 $\mu$s.
- 31.25 $\mu$s.
- 0.25 $ns$.
- 1.907 ms
19. An instruction is stored at location 550 with its address field at location 551. The address field has the value 2410. A processor register R1 contains the number 2310. What is the effective address if the addressing mode is direct?

a. 2962
b. 2410
c. 551
d. 4720

20. An instruction is stored at location 550 with its address field at location 551. The address field has the value 2410. A processor register R1 contains the number 2310. What is the effective address if the addressing mode is indexed?

a. 2962
b. 4720
c. 551
d. 2410

21. A two-word relative mode branch-type instruction is stored in memory at locations 207 and 208 (decimal). The branch is made to an address equivalent to decimal 195. Let the address field of the instruction (stored at address 208) be designated by X. What is the decimal value of X?

a. 1
b. -14
c. 14
d. -13

22. Add the two 8-bit numbers A=10110110 and B=00110111 that are given in 2's complement form. Determine the values of the C(Carry), Z(Zero), N(sign), and V(Overflow) status bits after the addition.

a. C=0, Z=0, N=0, V=1
b. C=0, Z=0, N=1, V=0
c. C=0, Z=0, N=0, V=0
d. C=1, Z=0, N=0, V=0
23. Consider the diagram in Figure 23. What kind of transfer is depicted by the diagram?

![Diagram](image)

a. Asynchronous transfer using strobing initiated by the destination.
b. Asynchronous transfer using handshaking initiated by the source.
c. Asynchronous transfer using handshaking initiated by the destination.
d. Asynchronous transfer using strobing initiated by the source.
24. Select the figure containing a program that evaluates the expression \( x=(a-b)\times(a+c)/(b-d) \) assuming a stack architecture.

<table>
<thead>
<tr>
<th>Figure 24.1</th>
<th>Figure 24.2</th>
<th>Figure 24.3</th>
<th>Figure 24.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUSH A</td>
<td>PUSH D</td>
<td>PUSH B</td>
<td>PUSH B</td>
</tr>
<tr>
<td>PUSH B</td>
<td>PUSH B</td>
<td>PUSH D</td>
<td>PUSH A</td>
</tr>
<tr>
<td>SUB</td>
<td>SUB</td>
<td>SUB</td>
<td>SUB</td>
</tr>
<tr>
<td>PUSH A</td>
<td>PUSH B</td>
<td>PUSH A</td>
<td>PUSH A</td>
</tr>
<tr>
<td>PUSH C</td>
<td>SUB</td>
<td>PUSH A</td>
<td>ADD</td>
</tr>
<tr>
<td>ADD</td>
<td>MUL</td>
<td>PUSH C</td>
<td>MUL</td>
</tr>
<tr>
<td>MUL</td>
<td>PUSH B</td>
<td>PUSH A</td>
<td>ADD</td>
</tr>
<tr>
<td>PUSH B</td>
<td>ADD</td>
<td>ADD</td>
<td>MUL</td>
</tr>
<tr>
<td>PUSH D</td>
<td>MUL</td>
<td>DIV</td>
<td>SUB</td>
</tr>
<tr>
<td>SUB</td>
<td>DIV</td>
<td>POP X</td>
<td>DIV</td>
</tr>
<tr>
<td>DIV</td>
<td>POP X</td>
<td>POP X</td>
<td>POP X</td>
</tr>
</tbody>
</table>

- a. Figure 24.1
- b. Figure 24.2
- c. Figure 24.4
- d. Figure 24.3

25. Select the figure containing a program that evaluates the expression \( x=(a+b-c)\times(d-e) \) assuming a register-to-register architecture with three-address instructions. The operand order for subtraction is difference, minuend, and subtrahend.

<table>
<thead>
<tr>
<th>Figure 25.1</th>
<th>Figure 25.2</th>
<th>Figure 25.3</th>
<th>Figure 25.4</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD R1,A</td>
<td>MOV T1,A</td>
<td>LD A</td>
<td>ADD R1,A,B</td>
</tr>
<tr>
<td>LD R2,B</td>
<td>ADD T1,B</td>
<td>ADD B</td>
<td>SUB R1,R1,C</td>
</tr>
<tr>
<td>LD R3,C</td>
<td>SUB T1,C</td>
<td>SUB C</td>
<td>SUB R2,D,E</td>
</tr>
<tr>
<td>LD R4,D</td>
<td>MOV T2,D</td>
<td>ST T1</td>
<td>MUL R1,R1,R2</td>
</tr>
<tr>
<td>LD R5,E</td>
<td>SUB T2,E</td>
<td>LD D</td>
<td>MOV X,R1</td>
</tr>
<tr>
<td>ADD R1,R1,R2</td>
<td>MUL T1,T2</td>
<td>SUB E</td>
<td></td>
</tr>
<tr>
<td>SUB R1,R1,R3</td>
<td>MOV X,T1</td>
<td>MUL T1</td>
<td></td>
</tr>
<tr>
<td>SUB R4,R4,R5</td>
<td>ST X,R1</td>
<td>ST X</td>
<td></td>
</tr>
</tbody>
</table>

- a. Figure 25.1
- b. Figure 25.2
- c. Figure 25.3
- d. Figure 25.4
26. An instruction is stored at location 550 with its address field at location 551. The address field has the value 2410. A processor register R1 contains the number 2310. What is the effective address if the addressing mode is relative?

a. 551
b. 2410
c. 2962
d. 4720

27. Find the average seek time, $T_s$, for a hard disk that rotates at 7200 rpm, has 512 tracks, 63 sectors per track, and 4096 bytes per sector and where the head can be moved from one track to another in 10$\mu$s.

a. 4.167 ms
b. 33.86 ms
c. 2.56 ms
d. 132.3 $\mu$s

28. Find the average rotational delay, $T_d$, for a hard disk that rotates at 7200 rpm, has 512 tracks, 63 sectors per track, and 4096 bytes per sector and where the head can be moved from one track to another in 10$\mu$s.

a. 4.167 ms
b. 132.3 $\mu$s
c. 33.86 ms
d. 2.56 ms

29. Find the disk transfer rate, $R_d$, by dividing the number of bytes in a sector by the time, $T_b$, required by the disk head to pass over the sector. $T_b$ can be computed by dividing the time needed by the disk to make one rotation by the number of sectors in a track.

a. $30.97 \times 10^6$ b/s
b. $251.7 \times 10^6$ b/s
c. $516.1 \times 10^3$ b/s
d. $1,858 \times 10^9$ b/s

30. Find the time required to copy a block of 1 MB ($2^{20}$ bytes) from hard drive to memory given that the disk is immediately ready to do so. The disk rotates at 7200 rpm. The disk drive contains a single platter and only one side of the platter is used. The head can be moved from one track to the next track in 10$\mu$s. There are 512 tracks, 63 sectors per track, and 4096 bytes per sector. The controller time is negligible.

a. 34.86 ms
b. 36.43 ms
c. 33.86 ms
d. 32.29 ms
31. Estimate the time required to transfer a block of 1 MB (2^{20} bytes) from hard drive to memory given that the disk rotates at 7200 rpm. The disk drive contains a single platter and only one side of the platter is used. The head can be moved from one track to the next track in 10 \mu s. There are 512 tracks, 63 sectors per track, and 4096 bytes per sector. The controller time is negligible.

a. 39.02 ms
b. 40.59 ms
c. 41.58 ms
d. 43.15 ms

32. A two-way set-associative cache in a system with 24-bit addresses has four 4-byte words per line and a capacity of 1 MB. Addressing is to the byte level. How many bits are there in the index?

a. 15
b. 16
c. 17
d. 18

33. A two-way set-associative cache in a system with 24-bit addresses has four 4-byte words per line and a capacity of 1 MB. Addressing is to the byte level. How many bits are there in the tag?

a. 6
b. 5
c. 4
d. 3

34. A two-way set-associative cache in a system with 24-bit addresses has four 4-byte words per line and a capacity of 1 MB. Addressing is to the byte level. Identify a valid index originating from one of the following main memory addresses in hexadecimal: F8C00F, 14AC89, 48CF0F, and 3ACF05.

a. 1801_{16}
b. 9591_{16}
c. 19E1_{16}
d. 2CF0_{16}
35. A two-way set-associative cache in a system with 24-bit addresses has four 4-byte words per line and a capacity of 1 MB. Addressing is to the byte level. How many of the given memory addresses can be in the cache simultaneously? Memory addresses are given in hexadecimal. The memory addresses are F8CF0f, 14AC89, 48CF0A, and C8CF05.

a. 1  
b. 2  
c. 3  
d. 4

36. How time is required to send 013F8FE0₁₆ on a bit-serial line using NRZI encoding given a 1 MHz clock?

a. 16 μs  
b. 17 μs  
c. 32 μs  
d. 34 μs
37. Select the NRZI waveform for the message 01FBF9\textsubscript{16}?

- **a.**

- **b.**

- **c.**

- **d.**

38. Find the effective access of a memory system consisting of a cache having an access speed of 1 \( ns \) and a main store having an access speed of 20 \( ns \) where the probability that the address referenced is in the cache is 0.97.

- a. 1.57 \( ns \)
- b. 2.54 \( ns \)
- c. 1.27 \( ns \)
- d. 2.38 \( ns \)
39. Find the effective access of a memory system consisting of a cache, main memory, and hard disk. The cache has an access time of $1 \text{ ns}$ and the probability that the addressed referenced is in cache is 0.98. The main store has an access time of $20 \text{ ns}$ and the probability that the address referenced is in main store is 0.999995. The hard disk has an access time of $10 \text{ ms}$.

   a. 1.57 $\text{ns}$  
   b. 2.54 $\text{ns}$  
   c. 1.27 $\text{ns}$  
   d. 2.38 $\text{ns}$

40. Find the physical address for the virtual address 0E45FB32 given a 32-bit virtual address where the most significant 20 bits are the virtual page number and the Translation Look-aside Buffer shown below.

<table>
<thead>
<tr>
<th>Tag (Virtual Page Number)</th>
<th>Data (Physical Page Number)</th>
</tr>
</thead>
<tbody>
<tr>
<td>01AF4</td>
<td>FFF</td>
</tr>
<tr>
<td>0E45F</td>
<td>E03</td>
</tr>
<tr>
<td>0123D</td>
<td>2F8</td>
</tr>
<tr>
<td>01A37</td>
<td>788</td>
</tr>
<tr>
<td>02BC4</td>
<td>48C</td>
</tr>
<tr>
<td>03CA0</td>
<td>657</td>
</tr>
</tbody>
</table>

   a. FFFB32  
   b. E03B32  
   c. 2F8B32  
   d. 788B32