8-3 A $64K \times 16$ RAM chip uses coincident decoding by splitting the internal decoder into row select and column select.

(a) Assuming that the RAM cell array is square, what is the size of the row decoder?

(b) Assuming that the RAM cell array is square, what is the size of the column decoder?

(c) Assuming that the RAM cell array is square, how many AND gates are required for decoding an address?

(d) Determine the row selection lines that are enabled when the input address in the binary equivalent of $(32000)_{10}$.

(e) Determine the column selection lines that are enabled when the input address in the binary equivalent of $(32000)_{10}$. 