1. Design a circuit that implements the state diagram shown.

![Symbolic State Diagram](image)

(a) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.
(b) Produce K-Maps for the next state decoder. Employ D Flip-Flops.
(c) Draw the logic diagram for the circuit.

2. Design a circuit that implements the state diagram shown.

![Symbolic State Diagram](image)

(d) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.
(e) Produce K-Maps for the next state decoder. Employ JK Flip-Flops.
(f) Draw the logic diagram for the circuit.

3. Design a circuit that will recognize the sequence 0111. The circuit samples an input line \( X \) on each rising-edge of the clock. The circuit raises the output signal \( Y = 1 \) when the sequence is recognized, otherwise, the output signal is set to zero \( (Y = 0) \). The circuit recognizes the sequence in any window of four clock pulses.

(a) Draw a block diagram of the circuit.
(b) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.
(c) Produce the K-Maps for the Next-State Decoder using D and JK Flip-Flops.
(d) Draw the logic diagram of the circuit using the decoder having the fewest gates.

4. Design a circuit that will recognize the sequence 110. The circuit samples an input line \( X \) on each rising-edge of the clock. The circuit raises the output signal \( Y = 1 \) when the sequence is recognized, otherwise, the output signal is set to zero \( (Y = 0) \). The circuit recognizes the sequence in any window of four clock pulses.

(a) Draw a block diagram of the circuit.
(b) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.
(c) Produce the K-Maps for the Next-State Decoder using D and JK Flip-Flops.
(d) Draw the logic diagram of the circuit using the decoder having the fewest gates.

5. Design a circuit that implement the state diagram shown. The circuit has one input signal $W$ and one output signal $Z$. Directed edges that designate state transitions are marked $W/Z$. Input signals can take on one of three symbols, 1, 0, or $x$. The symbol $x$ means that the directed edge is really two directed edges, one for $W = 1$, and the other for $W = 0$.

(a) Draw a block diagram of the circuit.
(b) Determine the number of Flip-Flops, assign states, and make a Present-State-Next-State Table.
(c) Produce the K-Maps for the Next-State Decoder using D and JK Flip-Flops.
(d) Draw the logic diagram of the circuit using the decoder having the fewest gates.